

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--|
| Power Supply Voltage | 16V |
| Power Dissipation (Package Limitation) | 1800 mW |
| Derate above $T_A = +25^\circ\text{C}$ | 15 mW/ $^\circ\text{C}$ |
| Operating Temperature Range (Ambient) | -40°C to $+85^\circ\text{C}$ |

| | |
|---------------------------------------|---|
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lamp Drive Voltage | |
| Max Voltage at Pin 7 with Lamp "Off" | 30V |
| Lamp Current | 100 mA |
| Blend Control Input Voltage (Pin 11) | 10V |
| Lead Temperature (Soldering, 10 sec.) | 260 $^\circ\text{C}$ |

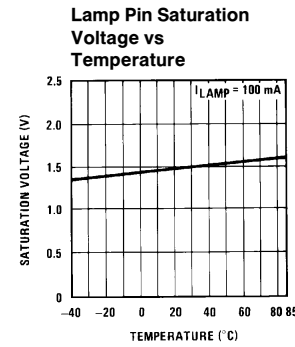
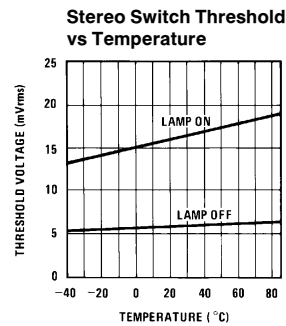
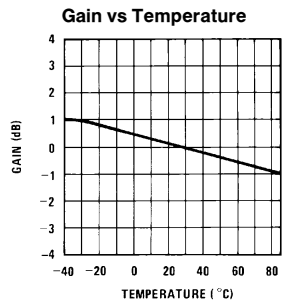
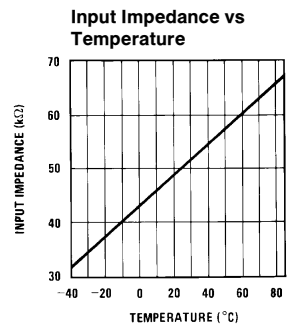
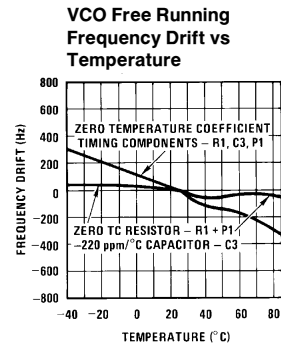
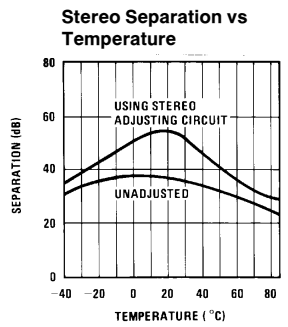
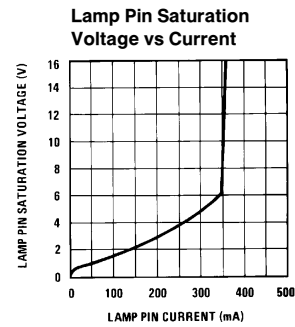
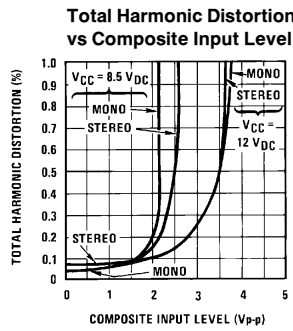
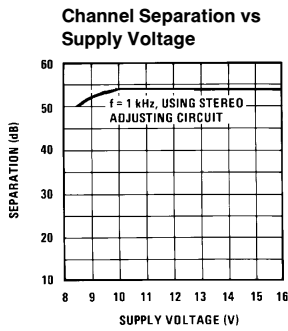
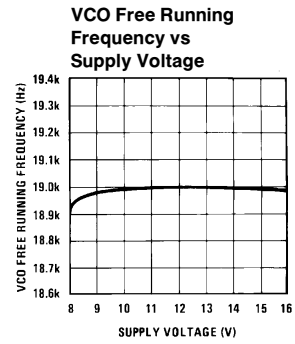
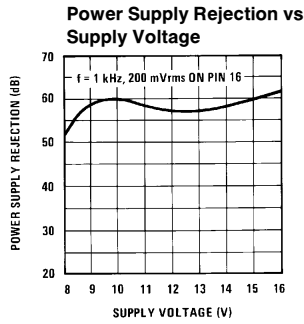
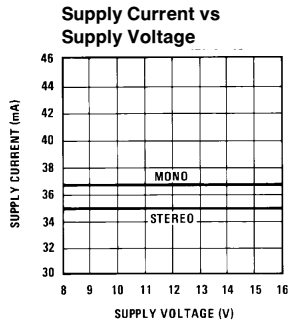
Electrical Characteristics Unless otherwise noted: $V_{CC} = 12 V_{DC}$, $T_A = 25^\circ\text{C}$, Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of *Figure 1*

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|-----|---------|------|------------------|
| Stereo Channel Separation | Unadjusted | 30 | | | dB |
| | Optimized on Other Channel (Note 1) | 40 | | | dB |
| Measured Voltage Gain (Note 1) | | 0.8 | 1 | 1.2 | |
| THD | 2.5 Vp-p Composite Input Signal | | 0.15 | 0.3 | % |
| | 1.5 Vp-p Composite Input Signal | | 0.08 | | % |
| Signal-to-Noise Ratio | DIN45405 Quasi Peak Reading rms 20 Hz-15 kHz | | 83 | | dB |
| | | | 88 | | dB |
| Ultrasonic Frequency Rejection | 19 kHz | | 31 | | dB |
| | 38 kHz | | 45 | | dB |
| Stereo Switch Level | 19 kHz Input Level for Lamp "On" | 12 | 16 | 20 | mVrms |
| Hysteresis | | | 8 | | dB |
| Output Voltage Change | With Mono/Stereo Switching (Note 2) | | 3 | 20 | mV _{DC} |
| Stereo Blend Control Voltage (Pin 11) (See <i>Figure 8</i>) | 3 dB Separation | | 0.7 | | V |
| | 30 dB Separation | | 1.7 | | V |
| Minimum Separation | Pin 11 at 0V | | | 1 | dB |
| Monaural Channel Imbalance | Pilot Tone Off | | 0.03 | 0.3 | dB |
| Sub-Carrier Harmonic Rejection | 76 kHz | | 80 | | dB |
| | 114 kHz | | 70 | | dB |
| | 152 kHz | | 83 | | dB |
| Supply Ripple Rejection | f = 1 kHz | | 57 | | dB |
| Input Impedance | | | 50 | | k Ω |
| Output Impedance | | | 100 | | Ω |
| Blend Control Current (Note 1) | | | -100 | -300 | μA |
| Capture Range | | | ± 4 | | % |
| Operating Supply Voltage | | 8 | | 16 | V |
| Current Drain | Lamp Disconnected | | 35 | | mA |

Note 1: See Applications Information and Circuit Description.

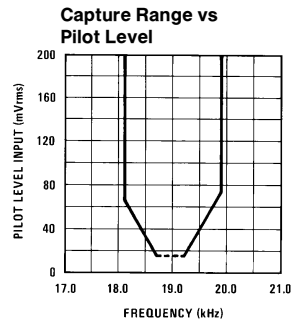
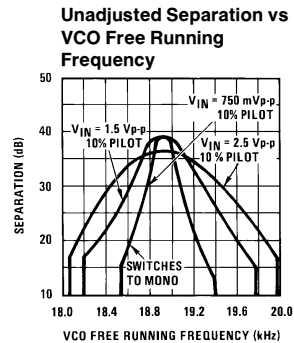
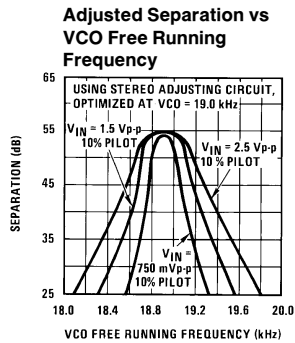
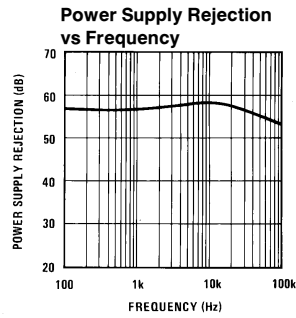
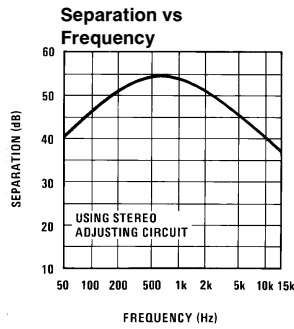
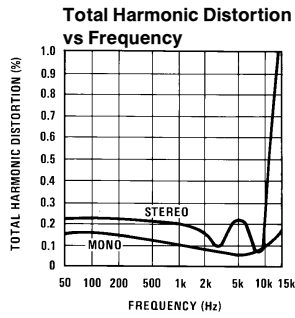
Note 2: This test is done with the stereo indicator lamp disconnected in order to remove DC shift due to thermal changes. These shifts have long time constants (100 ms) and therefore do not produce audible transients.

Typical Performance Characteristics



TL/H/7973-2

Typical Performance Characteristics (Continued)



TL/H/7973-3

Block Diagram

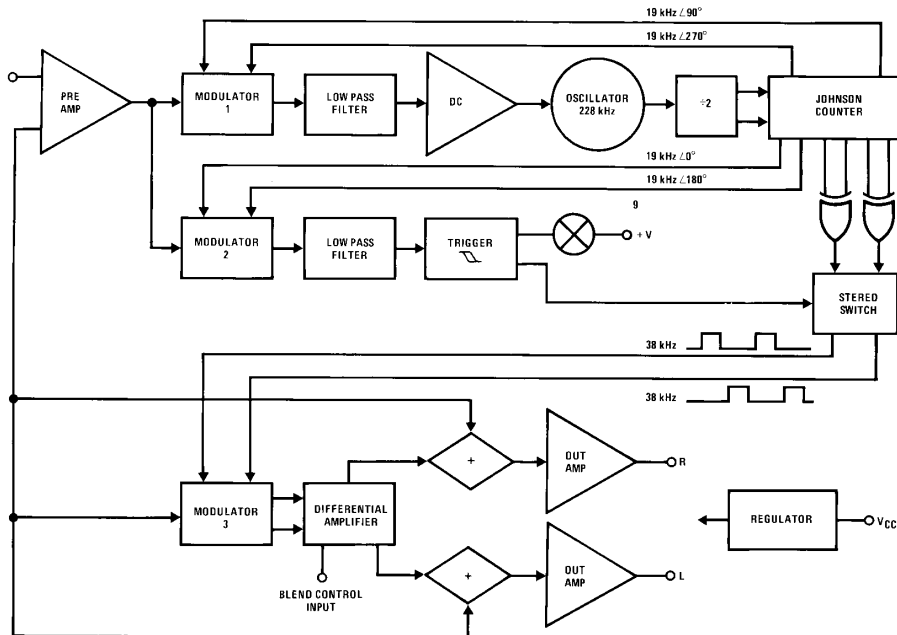


FIGURE 2

TL/H/7973-4

Circuit Description

INTRODUCTION

The LM4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic of the sub-carrier (114 kHz) excludes interference from the sidebands of adjacent transmitters, while the elimination of sensitivity to the third harmonic of the pilot tone (57 kHz) excludes interference from the ARI* system which employs this frequency.

CIRCUIT OPERATION

The block diagram of the circuit, shown in *Figure 2*, consists of three sections, the phase-lock-loop, including the digital waveform generator, the stereo switch, and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3-stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in *Figure 3*, which are used to drive the various modulators in the circuit, are developed.

*Auto Radio Information - used in Europe

The use of such drive waveforms produces the modulating functions also shown in *Figure 3*. The usual square waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The LM4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. LM1310).

The decoder section consists of a modulator (driven by the waveforms shown in *Figure 3*) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero; dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is deactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

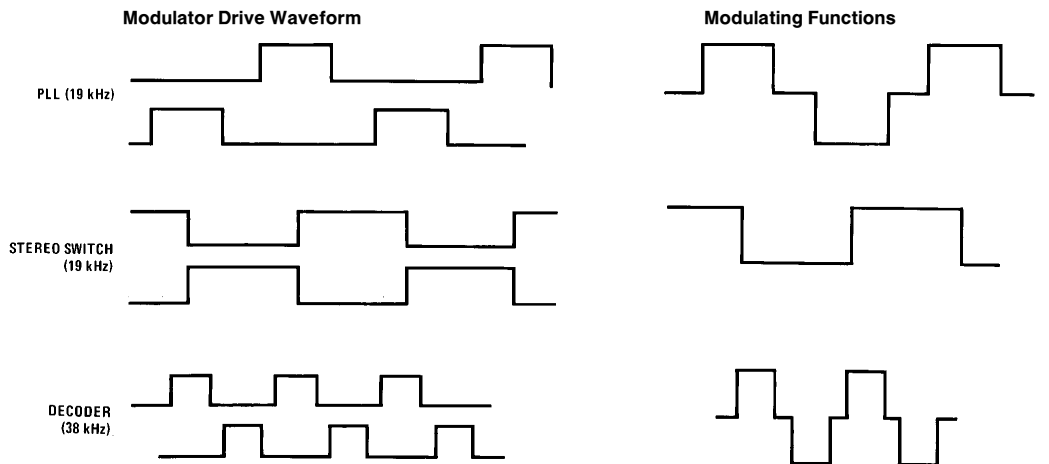


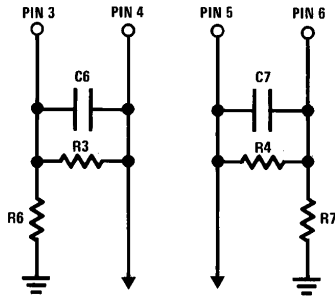
FIGURE 3. Digital Waveforms

TL/H/7973-5

Applications Information

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C5, R4, C7 of *Figure 1*) around the output amplifiers. The gain is unity when resistors of 5.1 k Ω are used. Higher gains may be obtained by using networks of the form shown in *Figure 4*.



TL/H/7973-6

FIGURE 4. Output Amplifier Feedback Networks

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 k Ω and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

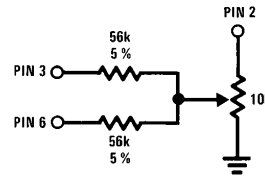
| Gain (dB) | R3, R4 | C6, C7 | | R6, R7 |
|-----------|----------------|------------|------------|---------------|
| | | 50 μ s | 75 μ s | |
| 0 | 5.1 k Ω | 10 nF | 15 nF | |
| 3 | 6.8 k Ω | 6.8 nF | 10 nF | 47k \pm 10% |
| 6 | 10k | 4.7 nF | 6.8 nF | 27k \pm 10% |

The maximum output level is 1 Vrms; consequently the max input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

A separation adjustment may be added, as shown in *Figure 5*, to compensate for the receiver's IF characteristics.

This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.



TL/H/7973-7

FIGURE 5. Networking Providing Adjustable Separation

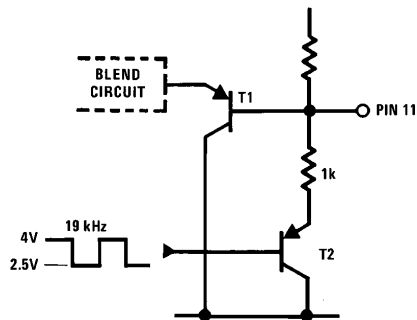
VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-Pin package the blend control has been combined with the 19 kHz output on Pin 11. The internal circuit providing this combination is shown in *Figure 6*.

If Pin 11 is left open-circuit the 19 kHz signal appears at a mean DC level of 4V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation the voltage on Pin 11 is reduced. At 3.2V T2 ceases conduction and the 19 kHz signal disappears.

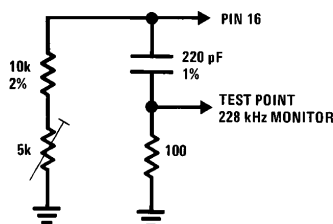
At 2.0V the blend circuit comes into operation and the separation decreases according to the curve shown in *Figure 8*.



TL/H/7973-8

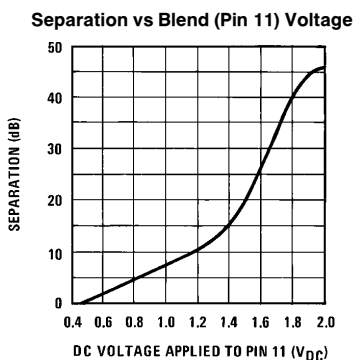
FIGURE 6. Blend Control Input Circuit

Applications Information (Continued)



TL/H/7973-9

FIGURE 7. Oscillator Network for Direct Frequency Measurement



TL/H/7973-10

FIGURE 8

Oscillator Tuning

If the variable separation facility is not required Pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as in *Figure 7*.

The output is a pulse train of approximately 1.5V amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g. car radio) the following component changes to *Figure 1* are recommended.

| | |
|-----------|-------------|
| R1 = 12k | C3 = 150 pF |
| R2 = 1.5k | C4 = 330 pF |
| R8 = 330 | C5 = 150 pF |
| P1 = 10k | |

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required the LM4500A can be forced into mono mode simply by grounding Pin 9 (see *Figure 1*). The 228 kHz oscillator will be automatically stopped.

The conditions governing mono/stereo switching on Pin 9 are the following:

Quiescent voltage: +2.3 V_{DC}

Current required to ensure mono operation (with 100 mVrms pilot level): 10 μA (from Pin 9 to ground)

Hysteresis: 0.7 μA

Stereo/mono switching & oscillator killing; less than +500 mV

Maximum stray capacitance between Pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS

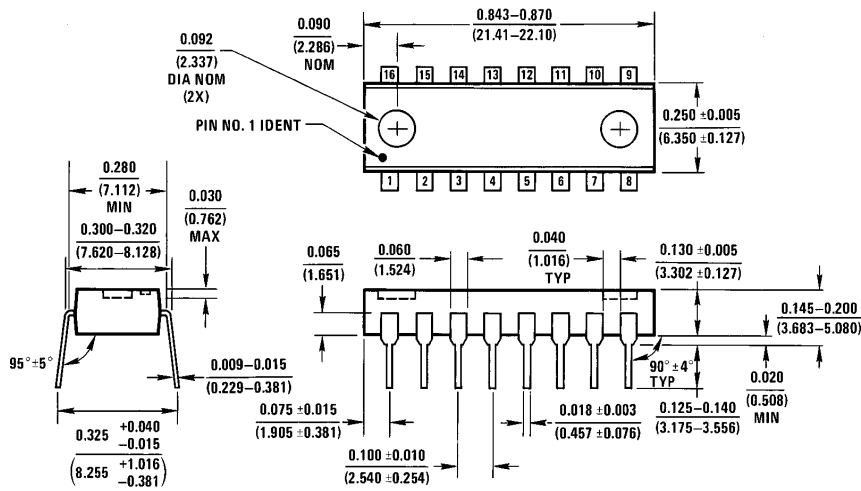
P1 19 kHz frequency adjustment.

P2 Channel separation adjustment and compensation for IF roll-off.

R3, R6 Gain fixing resistors. The values shown in the schematic are for unity gain.

C6, C7 De-emphasis capacitors. Value to give:
RC = 50 μs.

Physical Dimensions inches (millimeters)



**Dual-In-Line Package (N)
Order Number LN4500AN
NS Package Number N16A**

N16A (REV E)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: onjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
19th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.