National Semiconductor

DM5472/DM7472 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear, and Complementary Outputs

General Description

This device is a positive pulse triggered J-K master-slave flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the output on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

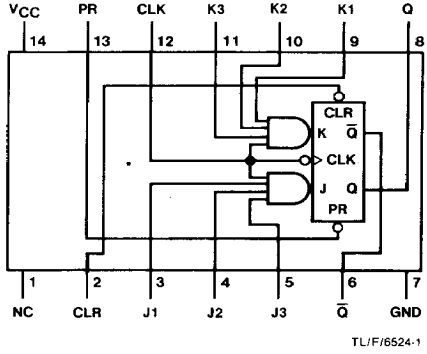
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6524-1

DM5472 (J) DM7472 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

Note 1: $J = (J1)(J2)(J3)$, $K = (K1)(K2)(K3)$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each positive clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM5472			DM7472			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge (↓) for falling edge.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	17	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		16	25	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: Clear is tested with preset high and preset is tested with clear high.