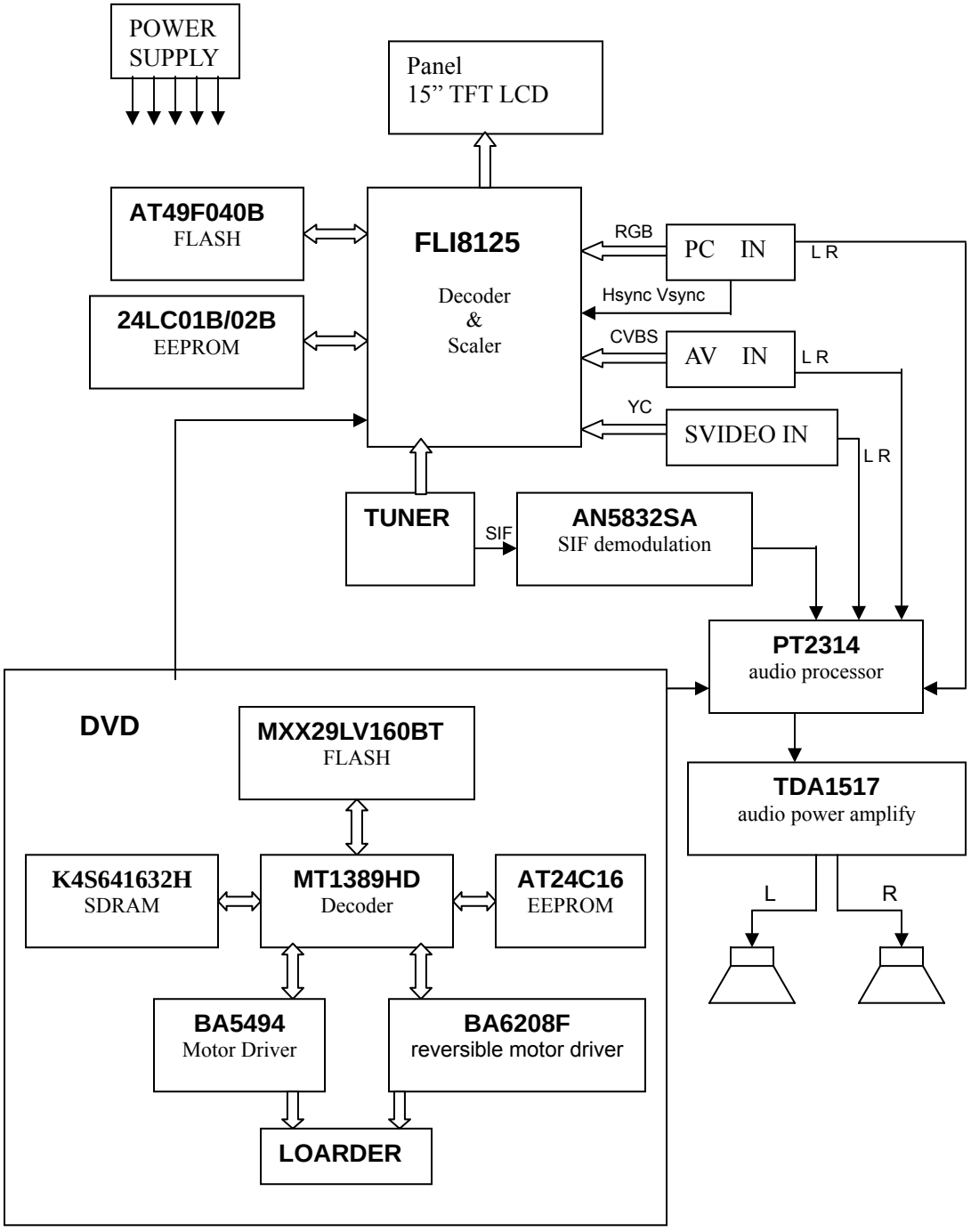
TEAC-LCDV1501M SERVICE MANUAL

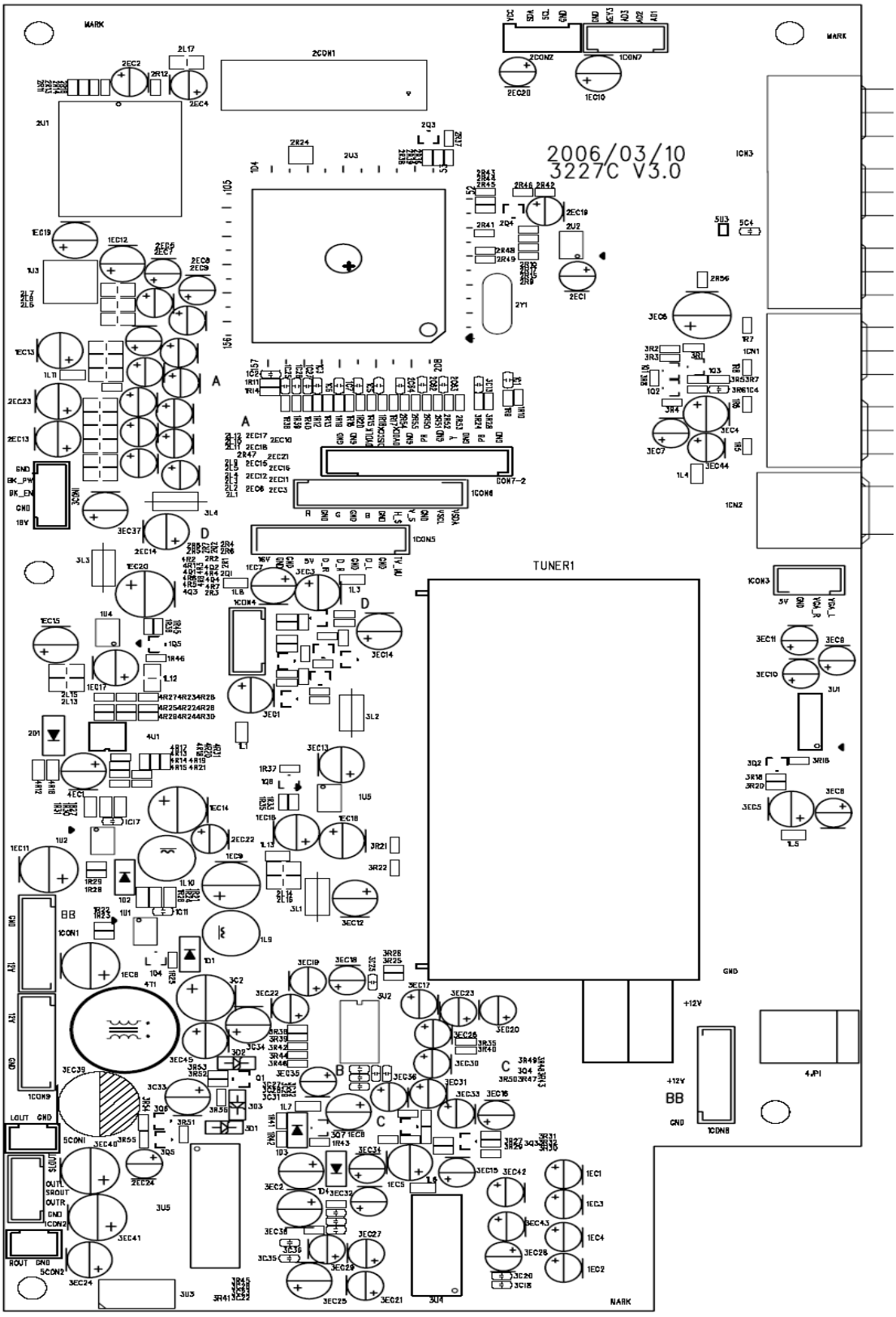
CONTENT

Part 1 Brief Introduction Of The TEAC-LCDV1501M

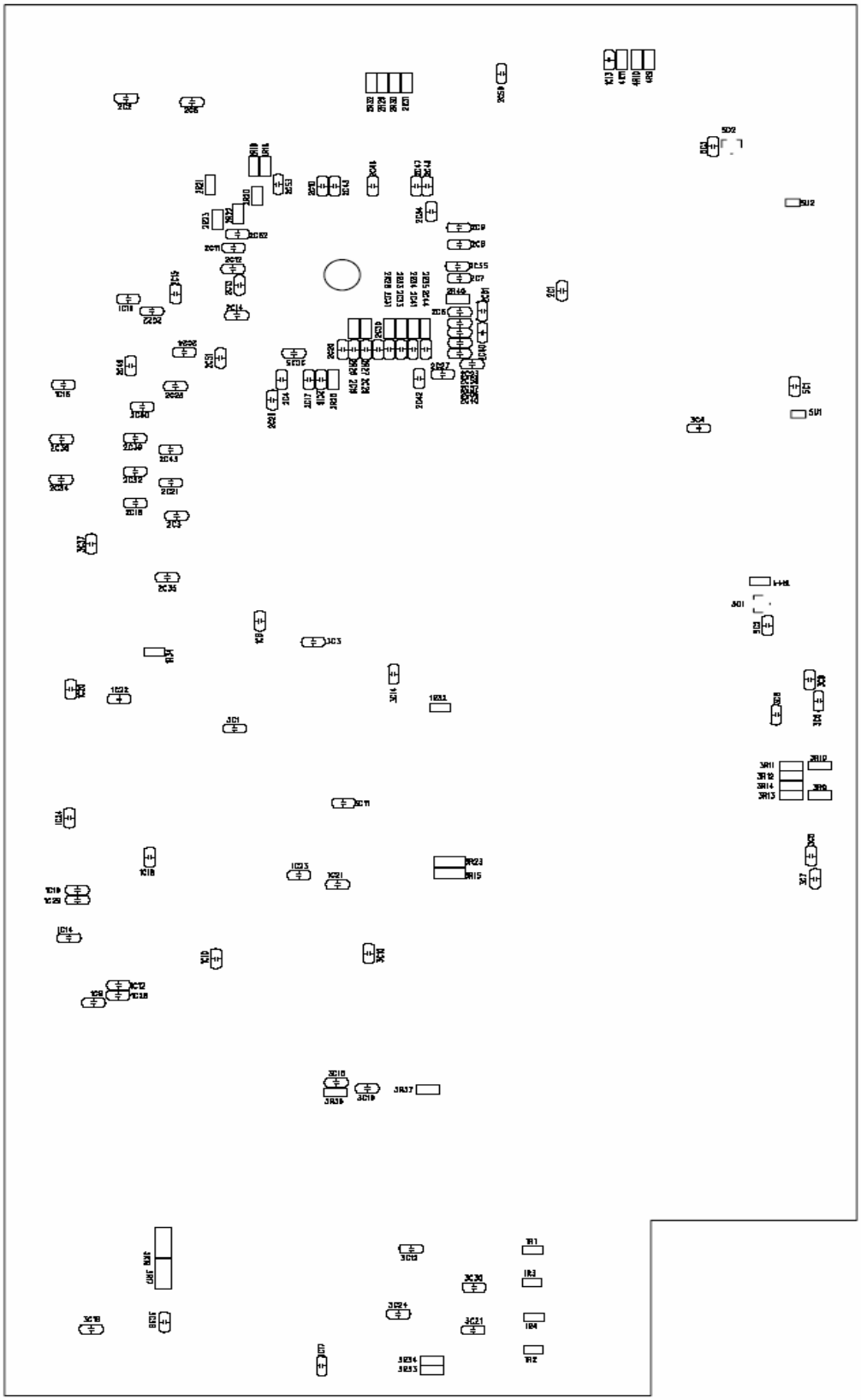
Thank you for buying Polaroid LCD-TV Product. As a high-resolution LCD-TV with a 15-inch screen, the TEAC-LCDV1501M incorporates DVD player, LCD display and TV receiver in one system. It adopts an MPEG2 decoding format to achieve horizontal resolution more than 500 lines. Designed with USB and SD/MS/MMC card port, it can be connected to USB device or SD/MS/MMC Card. It has several special functions such as sleep time setting, MTS support, auto TV searching and the picture enlargement. The product can not only be connected to external audio and video signal source and PC, but also features an AV output to extern audio and video device.

Specifications		
Brand	Polaroid TEAC-LCDV1501M	
TV Type	TV With LCD Screen	
Dimension		
Depth	176mm	
Height	374mm	
Width	388mm	
Weight	About 5.8 kg	
General		
Exterior Color	Black and Silver	
Screen Size	15 in.	
Number of Discs	1	
Video Inputs	AV, S-Video, Component, VGA	
Video Outputs	Composite	
Audio Inputs	L/R audio input(AV audio inputs share with S-Video and Component), PC audio input	
Laser wavelength	780/650 nm	
Video system	NTSC	
Frequency Response	20Hz-20KHz ± 2.5dB	
Audio signal-to noise rate	≥85 dB	
Audio distortion + noise	≤-70dB (1KHz)	
Dynamic range	≥80Db (1KHz)	
Channel separation	≥70Db (1KHz)	
Audio Out	Analog audio out	Out Level: $2V\pm^{0.2}_{1.0}$, Load: 10kΩ
	Digital audio out:	Out Level: $0.5V_{P-P}$, Load: 75Ω
Video Out	Out level: $1V_{P-P}$±0.2 load:75Ω Unbalanced negative	
Power Supply	AC 100-240V 50/60 Hz DC 12V 4A	
Power Consummation	＜48W	

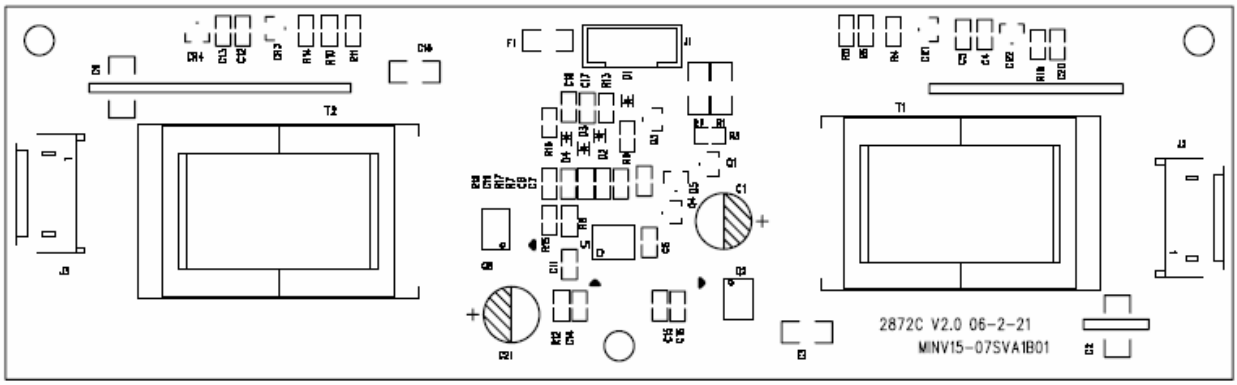

POWER SUPPLY
Panel
15” TFT LCD
AT49F040B
FLASH
FLI8125
Decoder
&
Scaler
24LC01B/02B
EEPROM
RGB
PC IN
L R
Hsync Vsync
CVBS
AV IN
L R
YC
SVIDEO IN
L R
TUNER
SIF
AN5832SA
SIF demodulation
PT2314
audio processor
DVD
MXX29LV160BT
FLASH
K4S641632H
SDRAM
MT1389HD
Decoder
AT24C16
EEPROM
BA5494
Motor Driver
BA6208F
reversible motor driver
LOARDER
TDA1517
audio power amplify
L
R



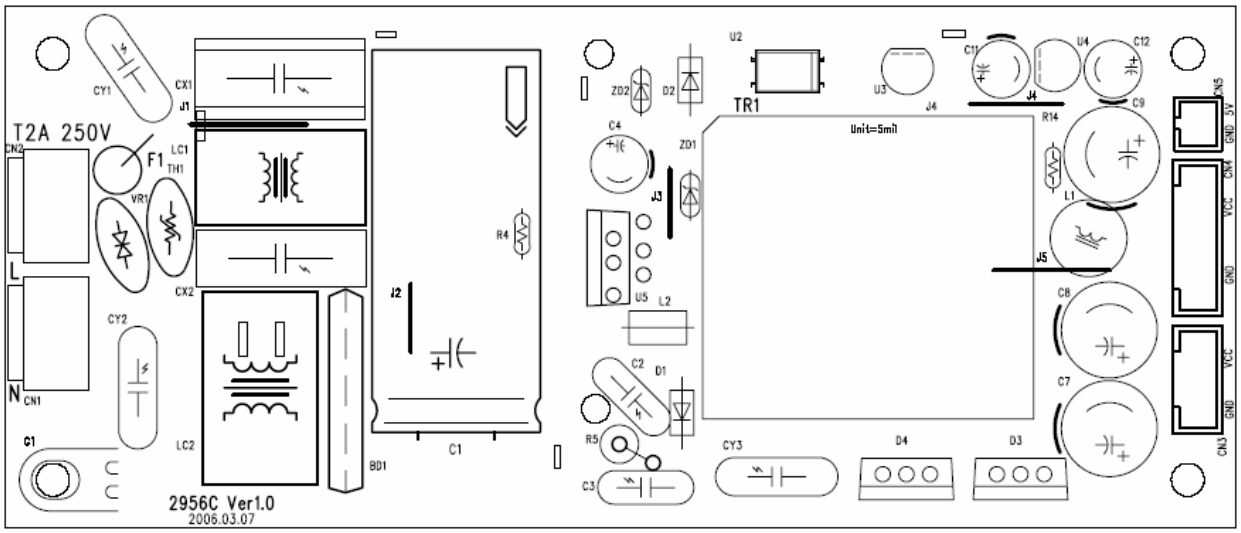
Main Board 3227C (Top View)



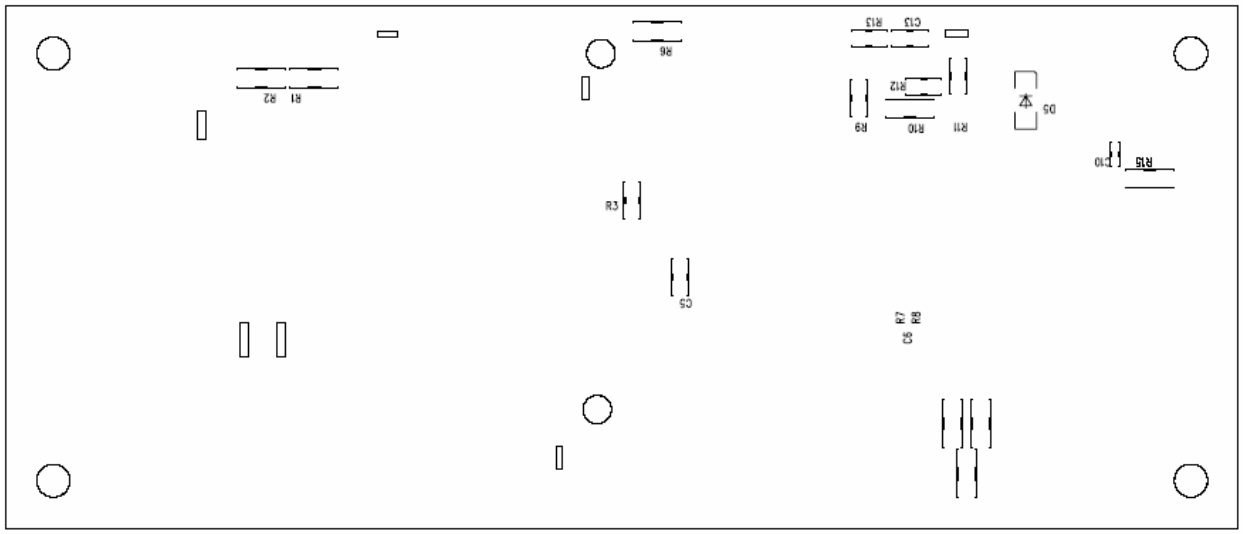
Main Board 3227C （Bottom view）



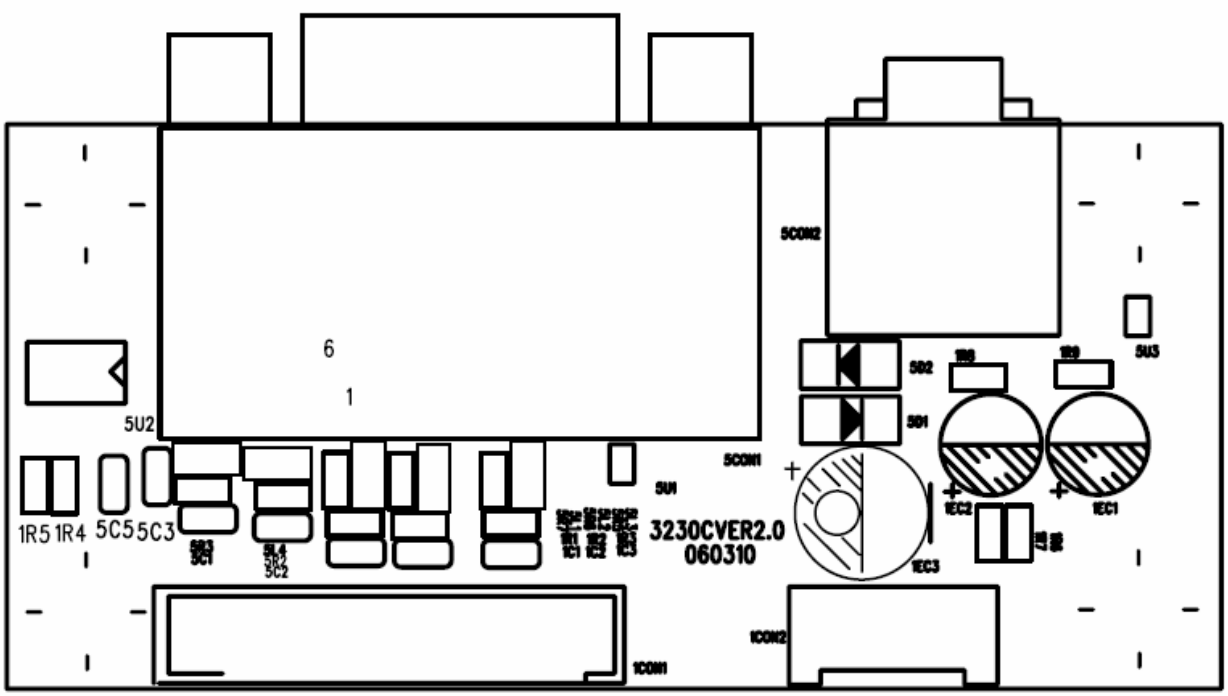
HI-voltage Board 2872C



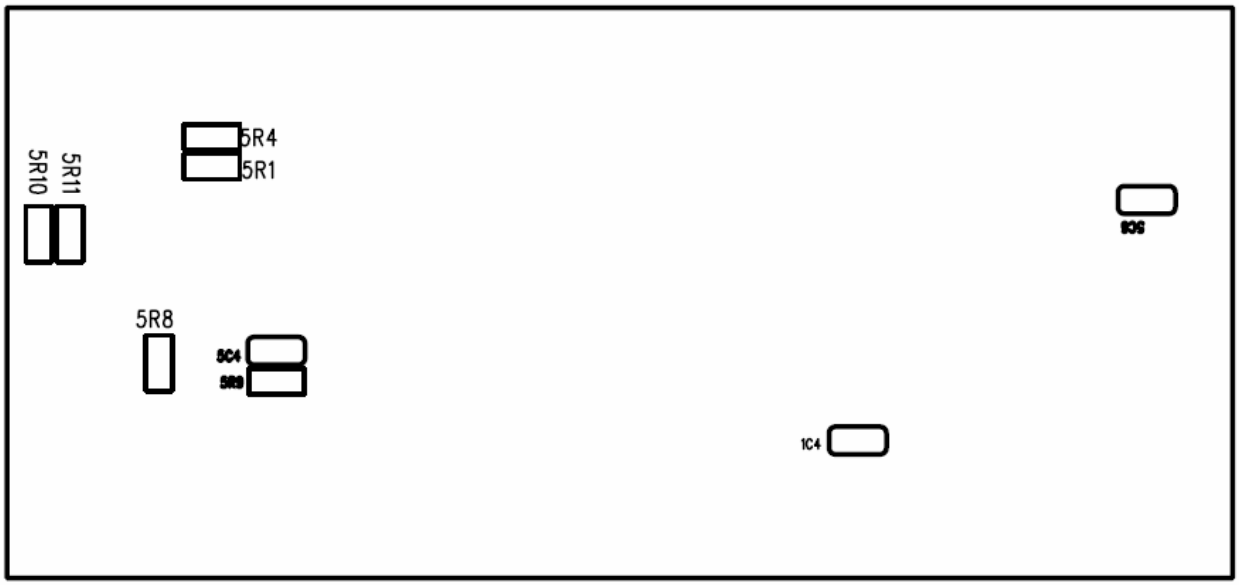
POWER Board 2956C (top view)



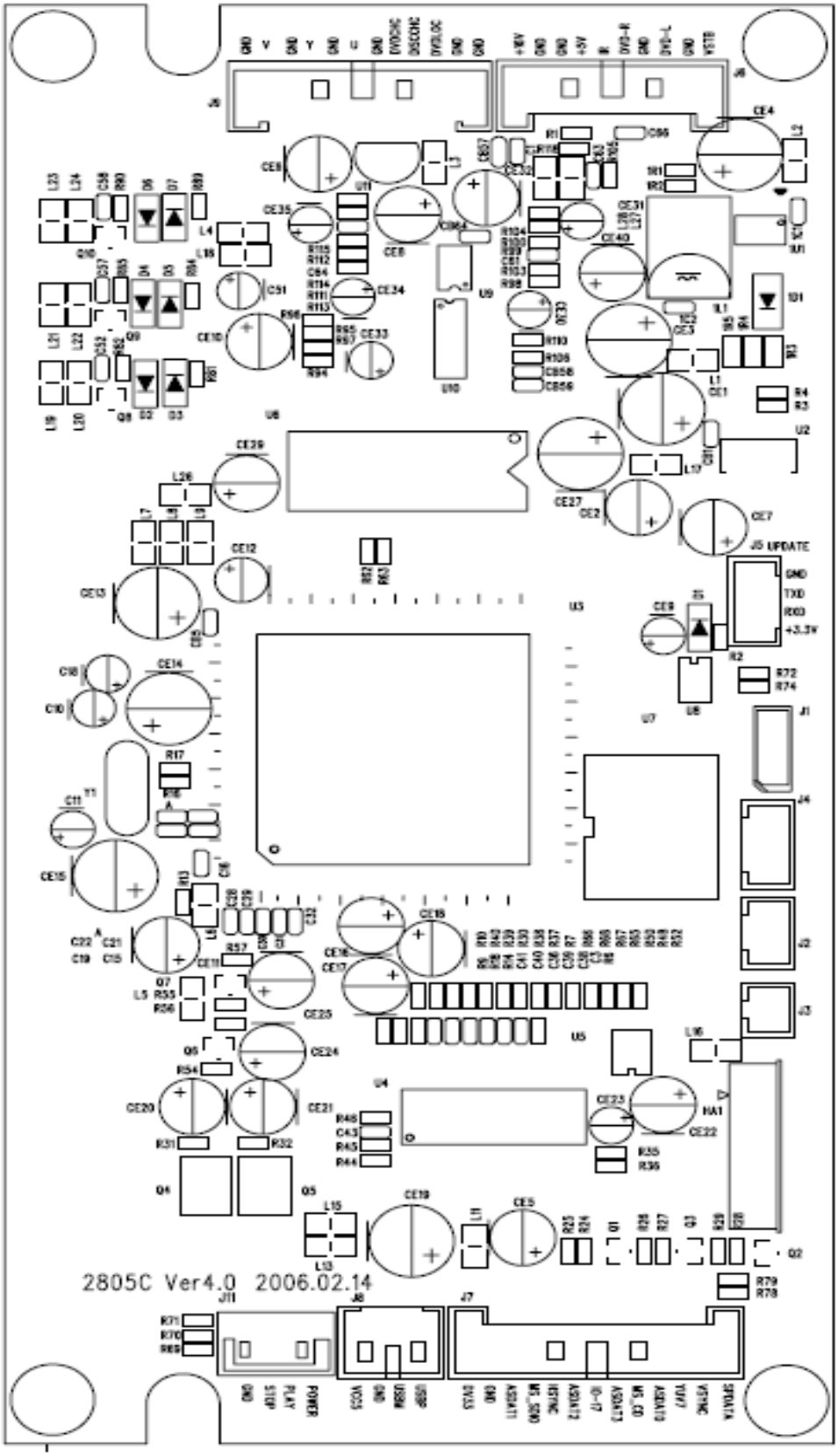
POWER Board 2956C (bottom view)



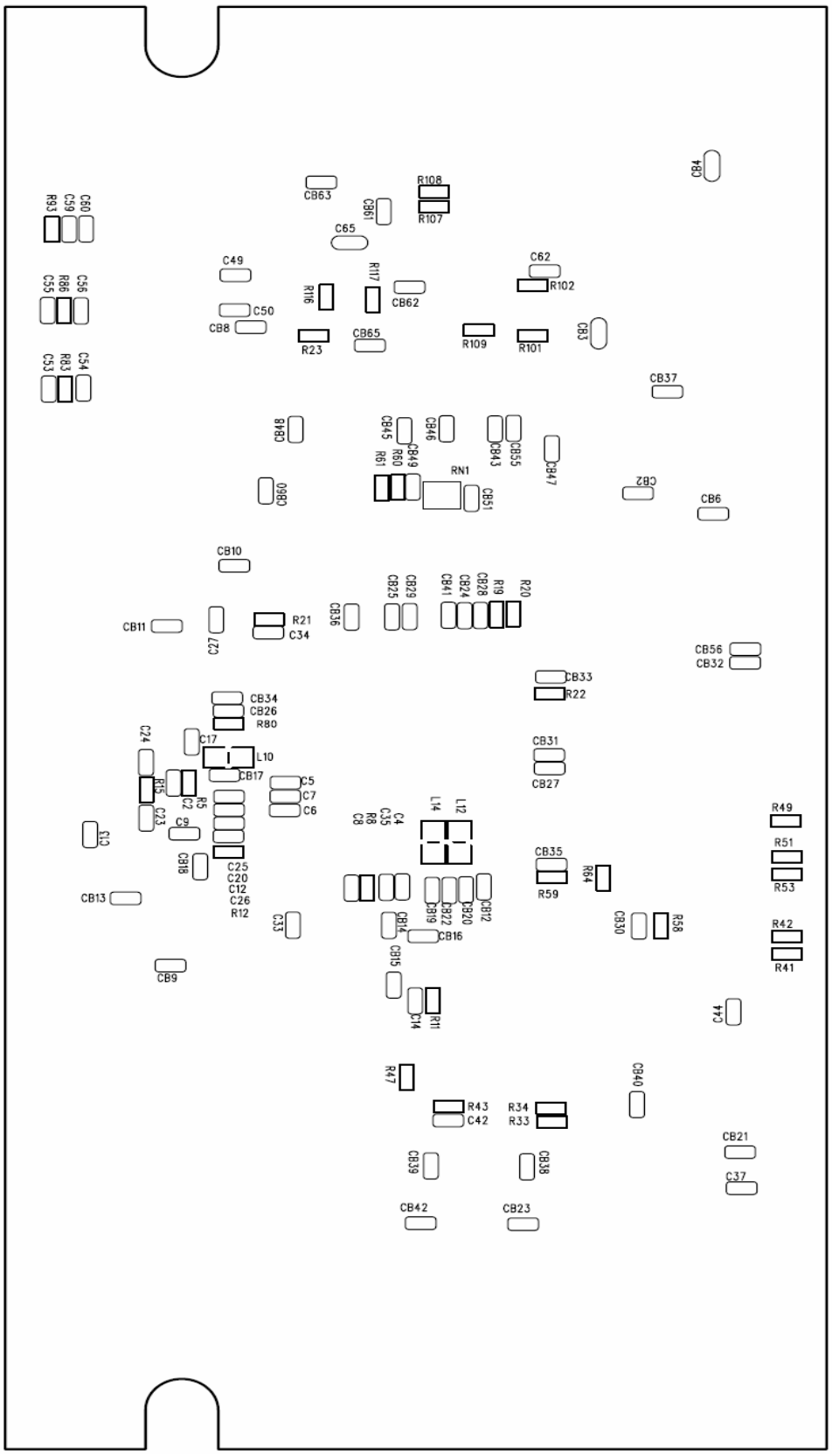
VGA Board 3230C(top view)



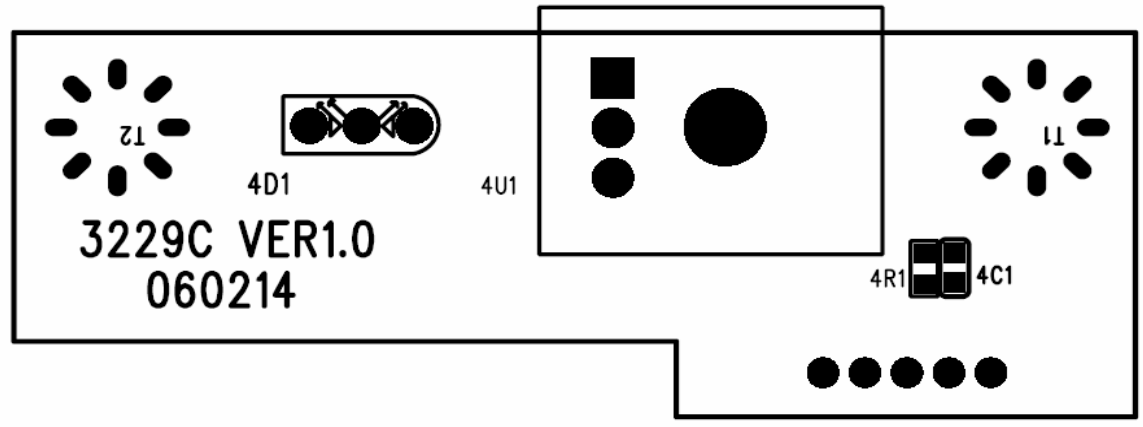
VGA Board 3230C(bottom view)



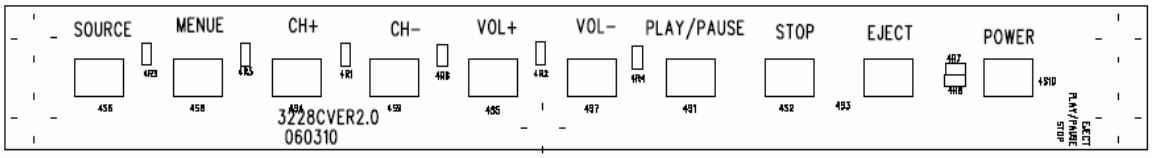
DVD Board 2805C(top view)



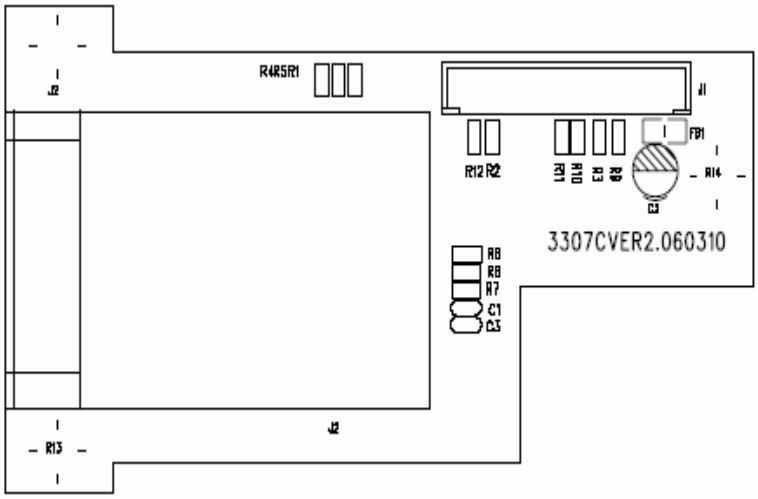
DVD Board 2805C(bottom view)



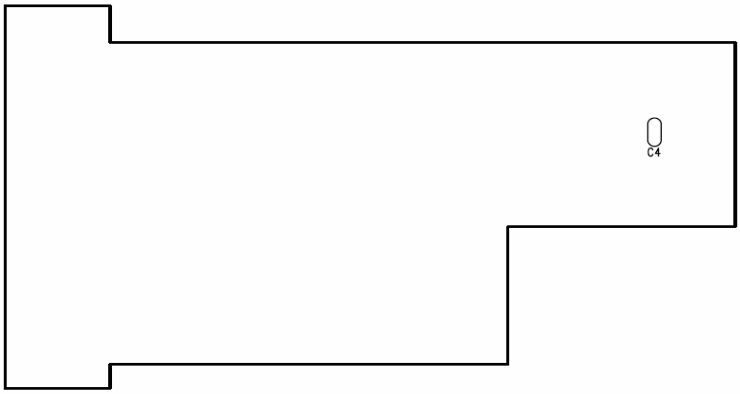
Remote Control Board 3229C



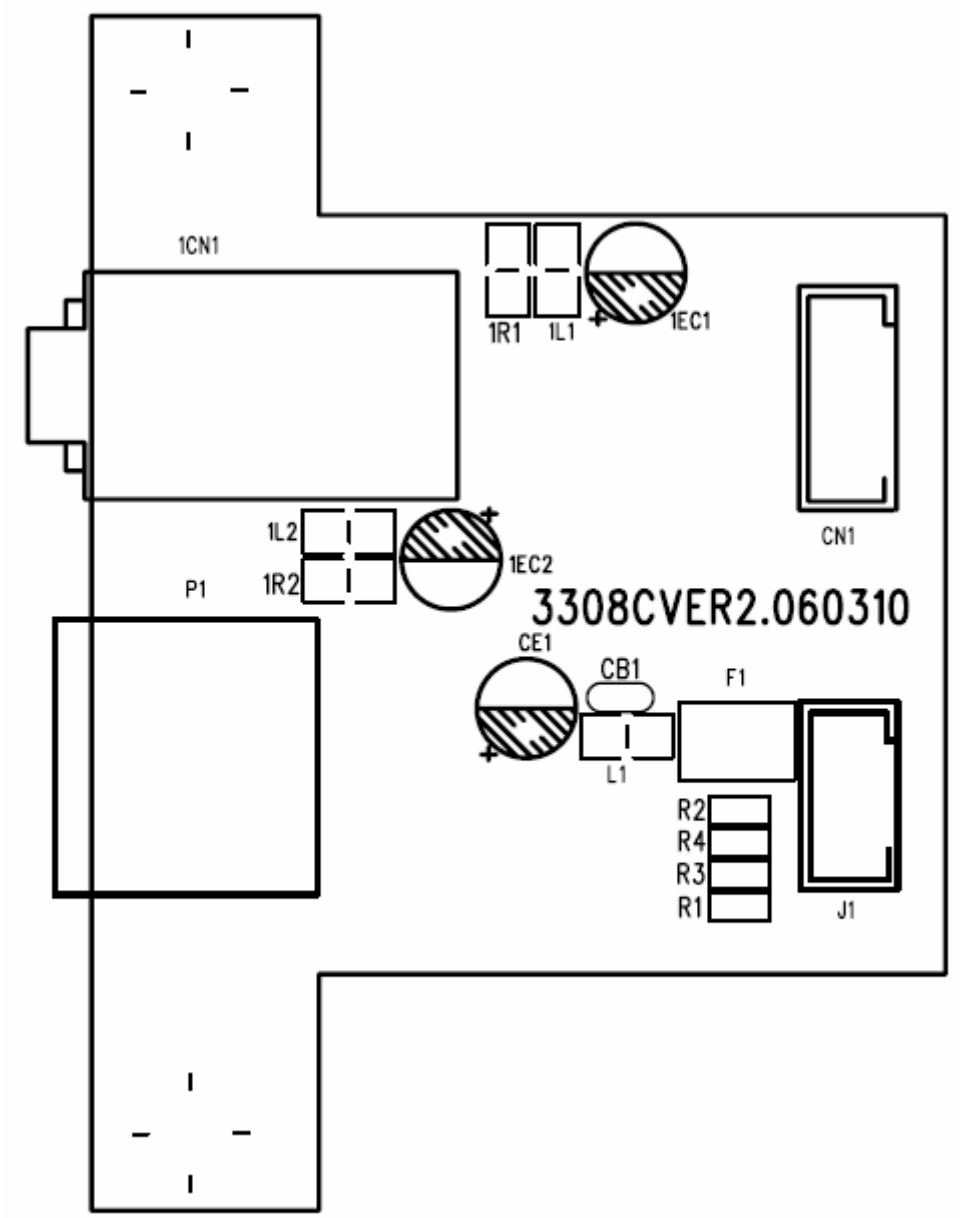
Key pad Board 3228C



Card Board 3307C(top view)



Card Board 3307C(bottom view)



USB and Headphone Board 3308C

Part 2 Key ICs And Assemblies

On Main Board			On DVD board		
Serial No	Position	Type	Serial no	Position	Type
1	1U1,1U2	AP1513	1	1U1	AP1513
2	1U3	LM1117	2	U2	LM1117
3	1U4,1U5	FDS9435A	3	U3	MT1389HD
4	2U1	AT49F040B	4	U4	BA5954
5	2U2	24LC01B/02B	5	U5	BA6208F
6	2U3	FLI8125	6	U6	K4S641632H
7	3U1	CD4052B	7	U7	MX29LV160BT
8	3U2	AN5832SA	8	U8	AT24C16
9	3U3	LM7809	9	U9	NJM4558
10	3U4	PT2314	10	U10	WM8714
11	3U5	TDA1517P			
On HI-voltage Board					
1	U1	BIT3193			
2	Q2,Q6	AP4511M			

ICS ON MAIN BOARD

1.AP1513

■ Features

- Input voltage: 3.6V to 18V.
- Output voltage: 0.8V to V_{CC}.
- Duty ratio: 0% to 100% PWM control
- Oscillation frequency: 300KHz typ.
- Soft-start, Current limit, Enable function
- Thermal Shutdown function
- Built-in internal SW P-channel MOS
- SOP-8L **Pb-Free** Package.

■ Applications

- PC Motherboard
- LCD Monitor
- Graphic Card
- DVD-Video Player
- Telecom Equipment
- ADSL Modem
- Printer and other Peripheral Equipment
- Microprocessor core supply
- Networking power supply

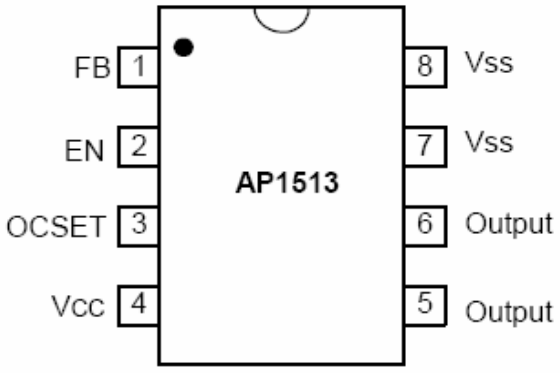
■ General Description

AP1513 consists of step-down switching regulator with PWM control. These devices include a reference voltage source, oscillation circuit, error amplifier, internal PMOS and etc.

AP1513 provides low-ripple power, high efficiency, and excellent transient characteristics. The PWM control circuit is able to very the duty ratio linearly from 0 up to 100%. This converter also contains an error amplifier circuit as well as a soft-start circuit that prevent s overshoot at startup. An enable function, an over current protect function and a short circuit protect function are built inside, and when OCP or SCP happens, the operation frequency will be reduced from 300KHz to 30KHz. Also, an internal compensation block is built in to minimum external component count.

With the addition of an internal P-channel Power MOS, a coil, capacitors, and a diode connected externally, these ICs can function as step-down switching regulators. They serve as ideal power supply units for portable devices when coupled with the SOP–8L mini-package, providing such outstanding features as low current consumption. Since this converter can accommodate an input voltage of up to 18V, it is also ideal when operating via an AC adapter.

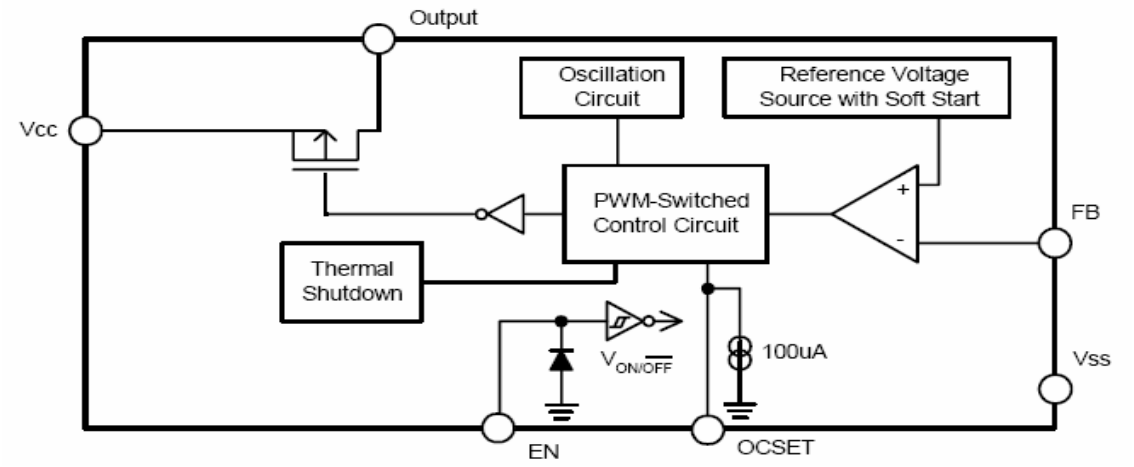
■ Pin Assignments



■ Pin Descriptions

Name	Pin	Description
FB	1	Feedback pin.
EN	2	Power-off pin H: Normal operation (Step-down operation) L: Step-down operation stopped (All circuits deactivated)
OCSET	3	Add an external resistor to set max output current.
Vcc	4	IC power supply pin
Output	5、6	Switch Pin. Connect external inductor/diode here. Minimize trace area at this pin to reduce EMI.
Vss	7、8	GND Pin

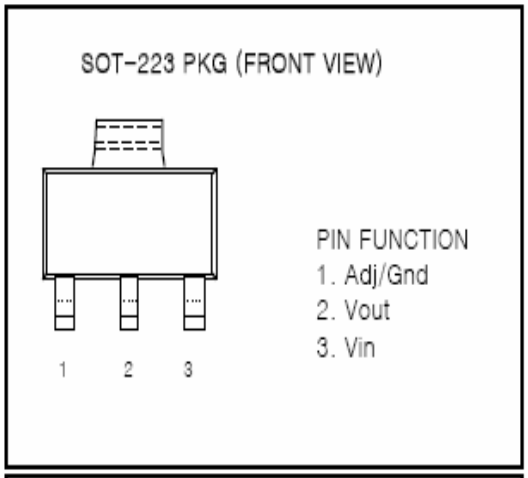
• **Block Diagram**

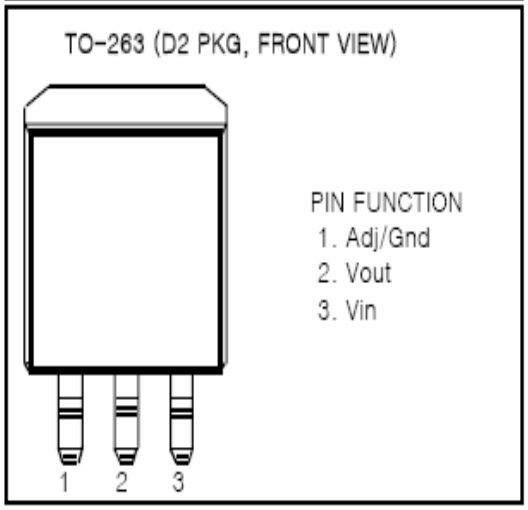


2.LM1117

FEATURES

- Output Current up to 1 A
- Low Dropout Voltage (700mV at 1A Output Current)
- Three Terminal Adjustable or Fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- 2.85V Device for SCSI-II Active Terminator
- 0.04% Line Regulaion, 0.1% Load Regulation
- Very Low Quiescent Current
- Internal Current andTerminal Limit
- Logic-Controlled Electronics Shutdown
- Surface Mount Package SOT-223 & TO-263 (D2-Pack)
- 100% Thermal Limit Burn-In





APPLICATION

- Active SCSI Terminators
- Portable/Plan Top/Notebook Computers
- High Efficiency Linear Regulators
- SMPS Post Regulators
- Mother B/D Clock Supplies
- Disk Drives
- Battery Chargers

ORDERING INFORMATION

Device (Marking)	Package
LM1117S	SOT-223
LM1117S-XX	
LM1117T	TO-263 (D2)
LM1117T-XX	

(X=Output Voltage=1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V, Adjustable=AD)

DESCRIPTION

The LM1117 is a low power positive-voltage regulator designed to meet 1A output current and comply with SCSI-II specifications with a fixed output voltage of 2.85V. This device is an excellent choice for use in battery-powered applications, as active terminators for the SCSI bus, and portable computers.
The LM1117 features very low quiescent current and very low dropout voltage of 700mV at a full load and lower as output current decreases. LM1117 is available as an adjustable or fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 5.0V output voltages.
The LM1117 is offered in a 3-pin surface mount package SOT-223 & TO-263. The output capacitor of 10μF or larger is needed for output stability of LM1117 as required by most of the other regulator circuits.

3.FDS9435A **Single P-Channel Enhancement Mode Field Effect Transistor**

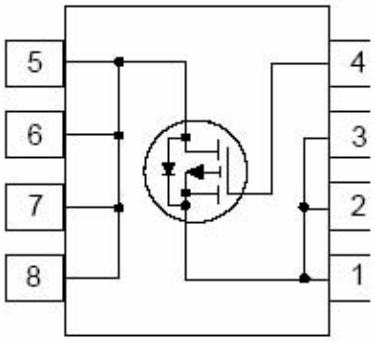
SO-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

• **Features**

-5.3 A, -30 V, $R_{DS(ON)}$ = 0.045 Ω @ V_{GS} = -10 V,
$R_{DS(ON)}$ = 0.075 Ω @ V_{GS} = - 4.5 V.

High density cell design for extremely low RDS(ON).

High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FDS9435A	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	-20	V
I_D	Drain Current - Continuous (Note 1a)	- 5.3	A
	- Pulsed	-50	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	°C/W

4.AT49F040B

- **Description**

The AT49F040B is a 5-volt-only in-system reprogrammable Flash Memory.Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology,the device offers access times to 55ns with power dissipation of just 110 mW over the commercial temperature range.

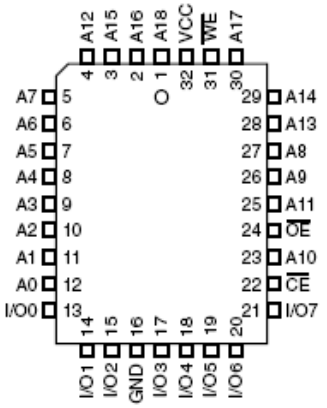
Features

- Single Supply for Read and Write: 4.5 to 5.5V
- Fast Read Access Time – 55 ns
- Internal Program Control and Timer
- Flexible Sector Architecture
  - One 16K Bytes Boot Sector with Programming Lockout
  - Two 8K Bytes Parameter Sectors
  - Eight Main Memory Sectors (One 32K Bytes, Seven 64K Bytes)
- Fast Erase Cycle Time – 8 Seconds
- Byte-by-Byte Programming – 12 µs/Byte Typical
- Hardware Data Protection
- $\overline{\text{DATA}}$ Polling or Toggle Bit for End of Program Detection
- Low Power Dissipation
  - 20 mA Active Current
  - 25 µA CMOS Standby Current
- Minimum 100,000 Write Cycles

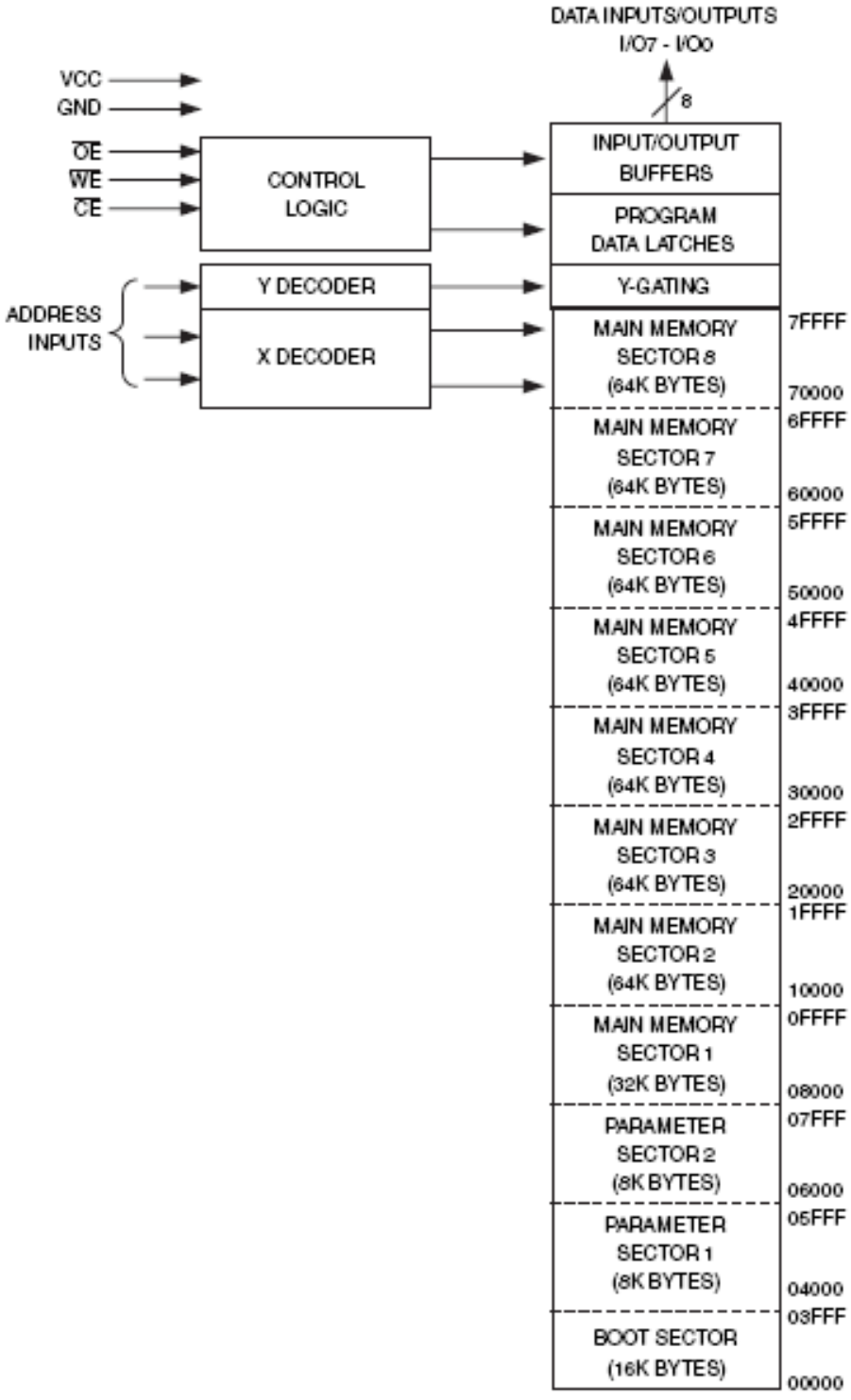
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

32-lead PLCC Top View



- **Block Diagram**

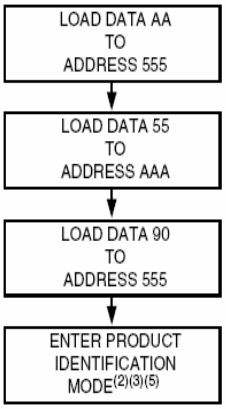


• Operating Modes

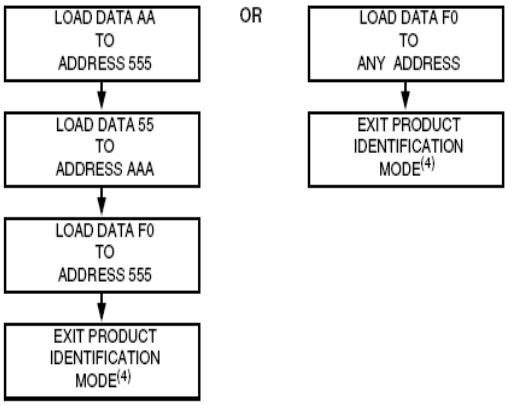
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program/Erase(2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H,(3), A0 = V_{IL}	Manufacturer Code(4)
				A1 - A18 = V_{IL}, A9 = V_H,(3), A0 = V_{IH}	Device Code(4)
Software(5)				A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code(4)
				A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code(4)

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 11.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 13H. Additional Device Code: 10H is read from address 0003H.
5. See details under Software Product Identification Entry/Exit down.

• Software Product Identification Entry(1)



• Software Product Identification Exit(1)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A11 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
   Additional Device Code is read for address 0003H
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 13H.
   Additional Device Code: 10H.

FEATURES

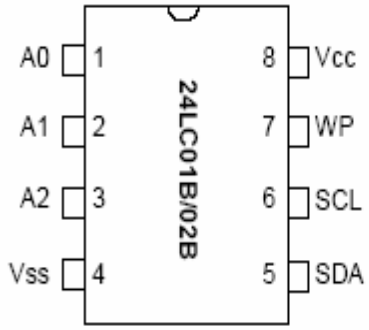
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 μA standby current typical at 5.5V
  - 5 μA standby current typical at 3.0V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400kHz (5.0V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 3,000V
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8 pin DIP or SOIC package
- Available for temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

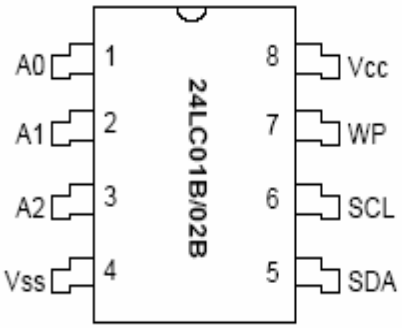
The Microchip Technology Inc. 24LC01B and 24LC02B are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 5 μA and 1 mA respectively. The 24LC01B and 24LC02B also have page-write capability for up to 8 bytes of data. The 24LC01B and 24LC02B are available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

PACKAGE TYPES

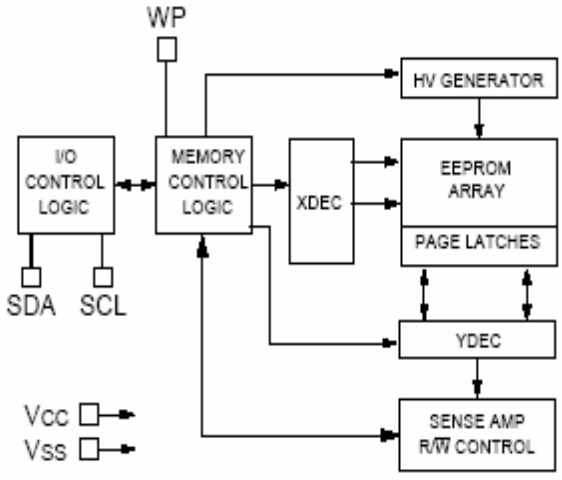
PDIP



SOIC



BLOCK DIAGRAM



The FLI8125 is a cost-effective, highly-integrated, mixed signal solution for TV and Digital Video applications. It incorporates a multi-standard video decoder, high-speed triple 8-bit Analog-to-Digital Converter(ADC),and front end switching. An integrated VBI Slicer adds Closed Captioning(CC) and Teletext service support, and the built-in microprocessor enables full system control without external devices.

Features

INTEGRATED TRIPLE ADC

- RGB / YPbPr support up to 135MHz
- SCART – RGB + Fast Blank support
- Interlaced and progressive scan
- External OSD support

DIGITAL INPUT PORT

- 24-bit re-configurable input port

INTEGRATED 2D VIDEO DECODER

- Worldwide NTSC/PAL/SECAM support
- Macrovision / VCR trick mode support

EMBEDDED MICROPROCESSOR

- Turbo 186 core
- Internal RAM / ROM
- Serial Flash / Parallel ROM support
- 2-wire slave controller, UART support
- Internal RESET Controller
- GPIOs , Low Bandwidth ADC – 6 input
- Infra-red Interface

SCALING ENGINE

- Independent H & V scaling factors
- 4:2:2 YPbPr or 4:4:4 RGB scaling
- Anamorphic scaling (non-linear)

FAROUDJA DCDI – EDGE™

- Edge Correction
  - – Eliminates objectionable stair-casing
  - – Enhances clarity and realism
- Horizontal Enhancement
- Adaptive Contrast and Color (ACC)
- Active Color Management - II (ACM-II)

DIGITAL OUTPUT

- 18/24-bit 85Mhz TTL output
- Dual LVDS up to SXGA
- Energy Spectrum Management for reducing EMI
- Programmable CLUT for gamma correction

OSD CONTROLLER

- Up to 4 windows: 1, 2 or 4-bits per pixel color
- Programmable Font scalar to meet Teletext requirements

VBI SLICER

- V-Chip, Closed Captioning, XDS, CGMS, WSS decode
- Teletext 1.5 support

JTAG SUPPORT

- Boundary Scan support

- **Pinout**

- **Pin List**

  I/O Legend: A = Analog, **I** = Input, **O** = Output, **P** = Power, **G=** Ground

Table 1: Analog Input Port

Pin Name	No.	I/O	Description
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
NC	159		No Connection. Leave this pin open for normal operation.
GND18_C	160	AG	Analog Ground (1.8V Return) for C channel. Must be directly connected to the analog system ground plane on board.
VDD18_C	161	AP	Analog Power (1.8V) for C Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
ADC_TEST	162	O	Analog Front End Test O/P. Leave this Pin open. Used for factory testing purpose only.
AVDD_ADC	163	AP	Analog Power (3.3V) for ADC. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AGND	164	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
AGND	165	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV1P	166	AI	Positive analog sync input for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	167	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.

A1P	168	AI	Positive analog input 'A' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	169	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B1P	170	AI	Positive analog input 'B' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	171	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C1P	172	AI	Positive analog input 'C' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_A	173	AP	Analog Power (3.3V) for ADC of Channel-A. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AN	174	AI	Negative analog input 'A' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-A Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	175	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV2P	176	AI	Positive analog sync input for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	177	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A2P	178	AI	Positive analog input 'A' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	179	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B2P	180	AI	Positive analog input 'B' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	181	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C2P	182	AI	Positive analog input 'C' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_B	183	AP	Analog Power (3.3V) for ADC of Channel-B. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
BN	184	AI	Negative analog input 'B' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-B Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	185	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV3P	186	AI	Positive analog sync input for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GNDS	187	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A3P	188	AI	Positive analog input 'A' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	189	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B3P	190	AI	Positive analog input 'B' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	191	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C3P	192	AI	Positive analog input 'C' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_C	193	AP	Analog Power (3.3V) for ADC of Channel-C. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
CN	194	AI	Negative analog input 'C' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-C Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	195	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV4P	196	AI	Positive analog sync input for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	197	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A4P	198	AI	Positive analog input 'A' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	199	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B4P	200	AI	Positive analog input 'B' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	201	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C4P	202	AI	Positive analog input 'C' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_SC	203	AP	Analog Power (3.3V) for ADC of SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
SVN	204	AI	Negative analog sync input for channels 1 through 4. This acts as the return Path for the Sources connected to SV Channel Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
VO_GND	205	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.

VOUT2	206	AO	Analog VOUT signal This is the Analog Video Output from the Decoder in the Composite Video format. This can be amplified and be fed to any video display device.
VDD18_SC	207	AP	Analog Power (1.8V) for SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GND18_SC	208	AG	Analog Ground (1.8V Return) for SYNC channel. Must be directly connected to the analog system ground plane on board.

Table 2: Low Bandwidth ADC Input Port

Pin Name	No	I/O	Description
VDDA33_LBADC	1	AP	Analog Power (3.3V) for Low Bandwidth ADC Block. Must be bypassed with 0.1uF capacitor.
LBADC_IN1	2	AI	Low Bandwidth Analog Input-1. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN2	3	AI	Low Bandwidth Analog Input-2. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN3	4	AI	Low Bandwidth Analog Input-3. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN4	5	AI	Low Bandwidth Analog Input-4. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN5	6	AI	Low Bandwidth Analog Input-5. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN6	7	AI	Low Bandwidth Analog Input-6. The Input signal connected to this Pin, must be bypassed with
LBADC_RTN	8	AG	This Pin provides the Return Path for LBADC inputs. Must be directly connected to the analog system ground plane on board.
VSSA33_LBADC	9	AG	Analog Ground for Low Bandwidth ADC Block. Must be directly connected to the analog system ground plane on board.

Table 3: RCLK PLL Pins

Pin Name	No	I/O	Description
GND_RPLL	11	DG	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD_RPLL_18	12	DP	Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to Ground Plane.
VBUFC_RPLL	13	O	Test Output. Leave this Pin Open. This is reserved for Factory Testing Purpose.
AGND_RPLL	14	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
XTAL	15	AO	Crystal oscillator output.
TCLK	16	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator.
AVDD_RPLL_33	17	AP	Analog Power (3.3V) for RCLK PLL. Must be bypassed with 0.1uF capacitor.

Table 4: Digital Video Input Port

Pin Name	No	I/O	Description
VID_CLK_1	153	I	Video port data clock input meant for Video Input – 1. Up to 75Mhz [Input, 5V-tolerant]
VIDIN_HS	122	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Horizontal Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Horizontal Sync Input for Video Input – 1. OR this Pin acts as Horizontal Sync Input for 24 Bit Video Input
VIDIN_VS	121	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Vertical Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Vertical Sync Input for Video Input – 1. OR this Pin acts as Vertical Sync Input for 24 Bit Video Input
VID_DATA_IN_0 VID_DATA_IN_1 VID_DATA_IN_2 VID_DATA_IN_3 VID_DATA_IN_4 VID_DATA_IN_5 VID_DATA_IN_6 VID_DATA_IN_7	135 136 137 138 139 140 141 142	IO	Input YUV data in 8-bit BT656 of Video Input – 1 [Bi-Directional, 5V-tolerant] OR Input Y Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Red Data in case of 24 Bit Video Input
Pin Name	**No**	**I/O**	**Description**

VID_DATA_IN_8 VID_DATA_IN_9 VID_DATA_IN_10 VID_DATA_IN_11 VID_DATA_IN_12 VID_DATA_IN_13 VID_DATA_IN_14 VID_DATA_IN_15	145 146 147 148 149 150 151 152	IO	Input Pr / Pb Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Green Data in case of 24 Bit Video Input
VID_DATA_IN_16 VID_DATA_IN_17 VID_DATA_IN_18 VID_DATA_IN_19 VID_DATA_IN_20 VID_DATA_IN_21 VID_DATA_IN_22 VID_DATA_IN_23	123 124 125 128 129 130 131 132	IO	Input Blue Data in case of 24 Bit Video Input OR Video Input – 2 in 8-bit with Embedded Sync / Separate Sync Sync in which case VID_DATA_IN_16 acts as the LSB of the 8-bit Video input and VID_DATA_IN_23 acts as the MSB of the 8-bit Video input.
VID_CLK2	118	I	Video port data clock input meant for Video Input – 2. Up to 75Mhz [Input, 5V-tolerant]
VID_DE/FLD	115	I	Video Active Signal Input or the Field Signal Input from external Digital Video Source.

Note: In case of Multiple Digital Video Input Sources, only one source could be in 8-Bit with embedded Sync (BT656 mode) format.

Table 5: System Interface

Pin Name	No	I/O	Description
RESETn	10	I	Hardware Reset (active low) [Schmitt trigger, 5v-tolerant] Connect to ground with 0.01uF (or larger) capacitor.
TEST	20	I	For normal mode of operation connect this Pin to Ground.
GPIO15	21	IO	This pin is available as a general-purpose input/output port. Also it is optionally programmable to give out the external chip select signal meant for external SRAM. Refer to note below.
HSYNC2	22	I	Horizontal Sync signal Input-2. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC2	23	I	Vertical Sync signal Input-2. Used when Analog RGB component signal carries separate VSYNC signal.
HOST_SCLK	24	IO	Host input clock or 186 UART Data In or JTAG clock signal. [Input, Schmitt trigger, 5V-tolerant]
HOST_SDATA	25	IO	Host input data or 186 UART Data Out or JTAG mode signal. [Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant]
DDC_SCLK	26	IO	DDC2Bi clock for VGA Port [internal 10K pull-up resistor]
DDC_SDATA	27	IO	DDC2Bi data for VGA Port [internal 10K pull-up resistor]
MSTR_SCLK	30	O	Clock signal from Master Serial 2 Wire Interface Controller
MSTR_SDATA	31	IO	Data signal meant for Master Serial 2 Wire interface Controller
TCK	34	IO	This Pin accepts the Input Clock signal in case of Boundary Scan Mode.
TDI	35	IO	This Pin accepts the Input Data signal in case of Boundary Scan Mode.
TMS	36	IO	This Pin accepts the Input Test Mode Select signal in case of Boundary Scan Mode.
TRST	37	IO	This Pin accepts the Boundary Scan Reset signal in case of Boundary Scan Mode.
GPIO6/IRin	38	IO	Input from Infra Red Decoder can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO7/IRQin	41	IO	Input Interrupt Request signal can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO8/IRQout	42	IO	This Pin will give out the Interrupt Signal to interrupt external Micro. When not used, this pin is available as General Purpose Input/output Port.
GPIO9/SIPC_SCLK	43	IO	This Pin accepts the Clock signal from External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. When not used, this pin is available as General Purpose Input/output Port.
GPIO10/SIPC_SDATA/ A18	44	IO	This Pin acts as the Data I/O signal when used with External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Or this Pin is programmable to give out Address # 18 from the Internal Micro when used with 512K External Memory. When not used, this pin is available as General Purpose Input/output Port.
GPIO11/PWM0	47	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO12/PWM1	48	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO13/PWM2	51	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
Pin Name	**No**	**I/O**	**Description**

GPIO14/PWM3/ SCART16	52	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Or it can be programmed to sense the Fast Blank Input signal from a SCART I/P source. When not used, this pin is available as General Purpose Input/output Port.
TDO	55	O	This Pin provides the Output Data in case of Boundary Scan Mode.
HSYNC1	156	I	Horizontal Sync signal Input-1. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC1	157	I	Vertical Sync signal Input-1. Used when Analog RGB component signal carries separate VSYNC signal.
101		O	Clock Output meant for External OSD Controller
102		O	Horizontal Sync Output meant for External OSD Controller
XOSD_CLK	103	O	Vertical Sync Output meant for External OSD Controller
XOSD_HS	104	O	Field Signal Output meant for External OSD Controller
PD20/B4/GPIO0 PD21/B5/GPIO1 PD22/B6/GPIO2 PD23/B7/GPIO3	86 87 88 89	IO	These Pins provide the Panel Data as shown in the TTL Display Interface Table below. These are available as General Purpose Input / Output Pins when not used as Panel Data.

Table 6: LVDS Display Interface

Pin Name	No	I/O	Description
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]
AVDD_LV_33	56	DP	Digital Power for LVDS Block. Connect to digital 3.3V supply.
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.
AVSS_LV	58	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	59	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_E	60	O	These form the Differential Data Output for Channel – 3 (Even).
CH3N_LV_E	61	O	
CLKP_LV_E	62	O	These form the Differential Clock Output Even Channel.
CLKN_LV_E	63	O	
CH2P_LV_E	64	O	These form the Differential Data Output for Channel – 2 (Even).
CH2N_LV_E	65	O	
CH1P_LV_E	66	O	These form the Differential Data Output for Channel – 1 (Even).
CH1N_LV_E	67	O	
CH0P_LV_E	68	O	These form the Differential Data Output for Channel – 0 (Even).
CH0N_LV_E	69	O	
AVSS_OUT_LV	70	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	71	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_O	72	O	These form the Differential Data Output for Channel – 3 (Odd).
CH3N_LV_O	73	O	
CLKP_LV_O	74	O	These form the Differential Clock Output Odd Channel.
CLKN_LV_O	75	O	
CH2P_LV_O	76	O	These form the Differential Data Output for Channel – 2 (Odd).
CH2N_LV_O	77	O	
CH1P_LV_O	78	O	These form the Differential Data Output for Channel – 1 (Odd).
CH1N_LV_O	79	O	
CH0P_LV_O	80	O	These form the Differential Data Output for Channel – 0 (Odd).
CH0N_LV_O	81	O	
AVSS_OUT_LV	82	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	83	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.

Table 7: TTL Display Interface

Pin Name	No	I/O	Description	
			For 8-bit panels	**For 6-bit panels**
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]	
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]	
AVDD_LV_33	56	DP	Digital Power for TTL Block. Connect to digital 3.3V supply.	
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.	
AVSS_LV	58	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	59	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
R0	60	O	Red channel bit 0 (Even)	Not used.
R1	61	O	Red channel bit 1 (Even)	Not used.
R2	62	O	Red channel bit 2 (Even)	Red channel bit 0 (Even)
R3	63	O	Red channel bit 3 (Even)	Red channel bit 1 (Even)
R4	64	O	Red channel bit 4 (Even)	Red channel bit 2 (Even)
R5	65	O	Red channel bit 5 (Even)	Red channel bit 3 (Even)
R6	66	O	Red channel bit 6 (Even)	Red channel bit 4 (Even)
R7	67	O	Red channel bit 7 (Even)	Red channel bit 5 (Even)
G0	68	O	Green channel bit 0 (Even)	Not used.
G1	69	O	Green channel bit 1 (Even)	Not used.
AVSS_OUT_LV	70	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	71	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
G2	72	O	Green channel bit 2 (Even)	Green channel bit 0 (Even)
G3	73	O	Green channel bit 3 (Even)	Green channel bit 1 (Even)
G4	74	O	Green channel bit 4 (Even)	Green channel bit 2 (Even)
G5	75	O	Green channel bit 5 (Even)	Green channel bit 3 (Even)
G6	76	O	Green channel bit 6 (Even)	Green channel bit 4 (Even)
G7	77	O	Green channel bit 7 (Even)	Green channel bit 5 (Even)
B0	78	O	Blue channel bit 0 (Even)	Not used.
B1	79	O	Blue channel bit 1 (Even)	Not used.
B2	80	O	Blue channel bit 2 (Even)	Blue channel bit 0 (Even)
B3	81	O	Blue channel bit 3 (Even)	Blue channel bit 1 (Even)
AVSS_OUT_LV	82	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	83	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
PD20/B4	86	O	Blue channel bit 4 (Even)	Blue channel bit 2 (Even)
PD21/B5	87	O	Blue channel bit 5 (Even)	Blue channel bit 3 (Even)
PD22/B6	88	O	Blue channel bit 6 (Even)	Blue channel bit 4 (Even)
PD23/B7	89	O	Blue channel bit 7 (Even)	Blue channel bit 5 (Even)
DEN	90	O	Display Data Enable	
DHS	91	O	Display Horizontal Sync.	
DVS	92	O	Display Vertical Sync.	
DCLK	93	O	Display Pixel Clock	
PD24	115	O	Red channel bit 0 (Odd)	Not used.

Pin Name	No	I/O	Description	
			For 8-bit panels	For 6-bit panels
PD25	114	O	Red channel bit 1 (Odd)	Not used.
PD26	113	O	Red channel bit 2 (Odd)	Red channel bit 0 (Odd)
PD27	112	O	Red channel bit 3 (Odd)	Red channel bit 1 (Odd)
PD28	111	O	Red channel bit 4 (Odd)	Red channel bit 2 (Odd)
PD29	110	O	Red channel bit 5 (Odd)	Red channel bit 3 (Odd)
PD30	109	O	Red channel bit 6 (Odd)	Red channel bit 4 (Odd)
PD31	108	O	Red channel bit 7 (Odd)	Red channel bit 5 (Odd)
PD32	107	O	Green channel bit 0 (Odd)	Not used.
PD33	106	O	Green channel bit 1 (Odd)	Not used.
PD34	105	O	Green channel bit 2 (Odd)	Green channel bit 0 (Odd)
PD35	104	O	Green channel bit 3 (Odd)	Green channel bit 1 (Odd)
PD36	103	O	Green channel bit 4 (Odd)	Green channel bit 2 (Odd)
PD37	102	O	Green channel bit 5 (Odd)	Green channel bit 3 (Odd)
PD38	101	O	Green channel bit 6 (Odd)	Green channel bit 4 (Odd)
PD39	123	O	Green channel bit 7 (Odd)	Green channel bit 5 (Odd)
PD40	124	O	Blue channel bit 0 (Odd)	Not used.
PD41	125	O	Blue channel bit 1 (Odd)	Not used.
PD42	128	O	Blue channel bit 2 (Odd)	Blue channel bit 0 (Odd)
PD43	129	O	Blue channel bit 3 (Odd)	Blue channel bit 1 (Odd)
PD44	130	O	Blue channel bit 4 (Odd)	Blue channel bit 2 (Odd)
PD45	131	O	Blue channel bit 5 (Odd)	Blue channel bit 3 (Odd)
PD46	132	O	Blue channel bit 6 (Odd)	Blue channel bit 4 (Odd)
PD47	118	O	Blue channel bit 7 (Odd)	Blue channel bit 5 (Odd)

Note: In case of 24 Bit TTL Panels the RGB Odd Channel Outputs will not be used. In that case they can be made available for other purposes as Address & Data from On-Chip Micro or Digital Video Input Data.

Table 8: Parallel/Serial ROM Interface

Pin Name	No	I/O	Description
A17	95	O	256K x8 PROM Address. These pins also have bootstrap functionality.
A16	96		For serial SPI ROM interface:
A15	100		- ROM_ADDR17 will be Serial Clock (ROM_SCLK)
A14	101		- ROM_ADDR16 will be Serial Data Output (ROM_SDO)
A13	102		For 512K X 8 PROM, Address Signal A18 is available thru Pin # 44 which is GPIO10.
A12	103		
A11	104		
A10	105		
A9	106		
A8	107		
A7	108		

A6 A5 A4 A3 A2 A1 A0	109 110 111 112 113 114 115		
D7 D6 D5 D4 D3 D2 D1 D0	132 131 130 129 128 125 124 123	IO	External PROM data input.
ROM_OEN	118	O	External PROM data Output Enable.
ROM_SDI/ ROM_WEN	97	O	External PROM data Write Enable (for In-System-Programming of FLASH) or Serial Data Input (SDI) for SPI ROM interface.
ROM_SCSN/ ROM_CSN	94	O	External PROM data Chip Select or Serial PROM Chip Select (ROM_SCSN) for SPI ROM interface.

Table 9: Digital Power and Ground

Pin Name	No	I/O	Description
RVDD_3.3	32 49 98 116 154	P	Ring VDD. Connect to digital 3.3V.
CVDD_1.8	18 28 39 45 84 119 126 133 143	P	Core VDD. Connect to digital 1.8V.
CRVSS	19 29 33 40 46 50 85 99 117 120 127 134 144 155	G	Chip ground for core and ring.

Table 10: JTAG Boundary Scan

Pin Name	No	I/O	Description
TCK	34	I	JTAG Boundary Scan TCK signal
TDO	55	O	JTAG Boundary Scan TDO signal
TDI	35	I	JTAG Boundary Scan TDI signal. Pad has internal 50K pull-up resistor.
TMS	36	I	JTAG Boundary Scan RST signal. Pad has internal 50K pull-up resistor.
TRST	37	I	JTAG Boundary Scan TMS signal. Pad has internal 50K pull-up resistor.

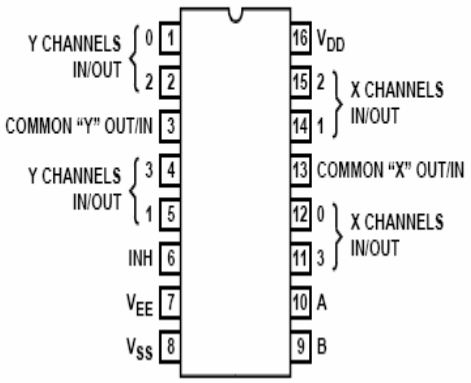
7.CD4052B

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

Features

- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . ≤20V_{P-P}
- Low ON Resistance, 125Ω (Typ) Over 15V_{P-P} Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to 20V_{P-P} (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Packag Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW



Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

• Pinouts

.

8.AN5832SA

- Silicon Monolithic Bipolar IC
- DIL 32-Pin Plastic Package (S0 Type)
- Demodulation of US TV sound multiplex input
- Function

  SIF demodulation

  Zenith TV sound multiplex decoder

  dbx TV noise reduction

  AGC (Automatic Gain Control)

- **Description of Test Circuit and Test Method**

No.	Parameter	Symbol	SW		Input Conditions	Measurement
			1	2		
1	Total circuit	I_{CC}	-	-	Vi(SIF)=90dBμV f=4.5MHz	Pin 19 current
2	Monaural output level	$V_{O(Mon)}$	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	AC voltmeter reading
3	Monaural frequency response 1	$V_{1(Mon)}$	b/c	a	(Monaural) 300Hz/1kHz, 30%mod 15kHz	Voltage ratio of 300Hz level to 1kHz level
4	Monaural frequency response 2	$V_{2(Mon)}$	b/c	a	(Monaural) 10Hz/1kHz, 30%mod 15kHz	Voltage ratio of 10kHz level to 1kHz level
5	Monaural Total Harmonic Distortion	$THD_{(Mon)}$	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	Distortion meter reading
6	Monaural S/N Ratio	$V_{n(Mon)}$	b/c	b	S:Monaural, 1kHz, 30%mod N:no signal CCIR filter, Q-PEAK response	AC voltmeter reading
7	L/R Channel Balance	$V_{LR(Mon)}$	b/c	a	(Monaural) 1kHz, 100%mod 15kHz	Voltage ratio of left-channel signal to right-channel signal
8	Stereo output level	$V_{O(st)}$	b/c	a	(L(R)-only) 1kHz, 100%mod 15kHz LPF	AC voltmeter reading
9	Stereo frequency response 1	$V_{1(st)}$	b/c	a	(L(R)-only) 300Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 300Hz level to 1kHz level
10	Stereo frequency response 2	$V_{2(st)}$	b/c	a	(L(R)-only) 10Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 10kHz level to 1kHz level
11	Stereo Total Harmonic Distortion	$THD_{(st)}$	b/c	a	(L(R)-only) 1kHz, 100%mod 15kHz LPF	Distortion meter reading
12	Stereo S/N Ratio	$V_{n(st)}$	b/c	b	S:L(R)-only, 1kHz, 30%mod N:Pilot signal CCIR filter, Q-PEAK response	AC voltmeter reading
13	Stereo Sensitivity	$V_{TH(st)}$	-	-	Pilot signal	Input level at stereo read resister comes to more than 3V.
14	Stereo hysteresis	$V_{HY(st)}$	-	-	Pilot signal	Input level at stereo read resister comes to less than 1.5V.
15	Stereo Separation 1	SEP1	b/c	a	(L(R)-only) 400Hz, 30%mod 15kHz LPF	Voltage ratio of left-channel signal to right-channel signal
16	Stereo Separation 2	SEP2	b/c	a	(L(R)-only) 2kHz, 30%mod 15kHz LPF	Voltage ratio of left-channel signal to right-channel signal
17	SAP output level	$V_{O(SAP)}$	b/c	a	(SAP) 1kHz, 100%mod 15kHz LPF	AC voltmeter reading
18	SAP frequency response 1	$V_{1(SAP)}$	b/c	a	(SAP) 300Hz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 300Hz level to 1kHz level
19	SAP frequency response 2	$V_{2(SAP)}$	b/c	a	(SAP) 8kHz/1kHz, 30%mod 15kHz LPF	Voltage ratio of 8kHz level to 1kHz level
20	SAP Total Harmonic Distortion	$THD_{(SAP)}$	b/c	a	(SAP) 1kHz, 100%mod 15kHz LPF	Distortion meter reading

21	SAP S/N Ratio	$V_{n(SAP)}$	b/c	b	S:(SAP) 1kHz, 30%mod N:SAP carrier signal CCIR filter, Q-PEAK response	AC voltmeter reading
22	SAP Sensitivity	$V_{TH(SAP)}$	-	-	SAP carrier signal	Input level at SAP read resister comes to more than 3V.
23	SAP Hysteresis	$V_{HY(SAP)}$	-	-	SAP carrier signal	Input level at SAP read resister comes to less than 1.5V.
24	SAP demodulation dynamic range 1	DSAPL	b	a	(SAP) fm=1kHz, fc=72kHz THD > 20%	Distortion meter reading
25	SAP demodulation dynamic range 2	DSAPH	b	a	(SAP) fm=1kHz, fc=85kHz THD > 20%	Distortion meter reading
26	SAP to stereo crosstalk	CT_1	b/c	a	(SAP) 1kHz, 100%mod (Stereo) Pilot signal 15kHz LPF	Ratio of AC voltmeter when St output select to VO(SAP)
27	Stereo to SAP crosstalk	CT_2	b/c	a	(Stereo) 1kHz, 100%mod (SAP) carrier signal 15kHz LPF	Ratio of AC voltmeter when SAP output select to VO(St)
28	SAP to monaural crosstalk	CT_3	b/c	a	(SAP) 1kHz, 100%mod 15kHz LPF	Ratio of AC voltmeter when Mono output select to VO(SAP)
29	Monaural to SAP crosstalk	CT_4	b/c	a	(Monaural) 1kHz, 100%mod (SAP) carrier signal 15kHz LPF	Ratio of AC voltmeter when SAP output select to VO(Mon)
30	AGC Gain 1	V_{AGC1}	b/c	a	(Monaural) 1kHz, 10%mod 15kHz LPF	AC voltmeter reading
31	AGC Gain 2	V_{AGC2}	b/c	a	(Monaural) 1kHz, 100%mod 15kHz LPF	AC voltmeter reading

- **Pin Description**

Pin No.	Function	Pin No.	Function
1	N.C.	21	SIF IN
2	Wide Band Timing	22	SIF REF
3	Wide Band DET	23	STEREO REF
4	Spectral Timing	24	SDA/SAPID
5	Spectral DET	25	Ground
6	Spectral Filter	26	PE
7	I^2C/Parallel SW	27	SCL/STID
8	AGC SW	28	AGC DET
9	MODE SW	29	Right-channel output
10	Force Monaural SW	30	Left-channel output
11	Mute SW	31	N.C.
12	SIF/Base Band SW	32	L-R REF
13	SAP Noise DET		
14	SAP DET		
15	L+R REF		
16	N.C.		
17	Pilot DET		
18	Stereo PLL Filter		
19	V_{CC}		
20	N.C.		

9.LM7809

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.5 ampere.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

FEATURES

- Output Current in Excess of 1.5 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% Tolerance

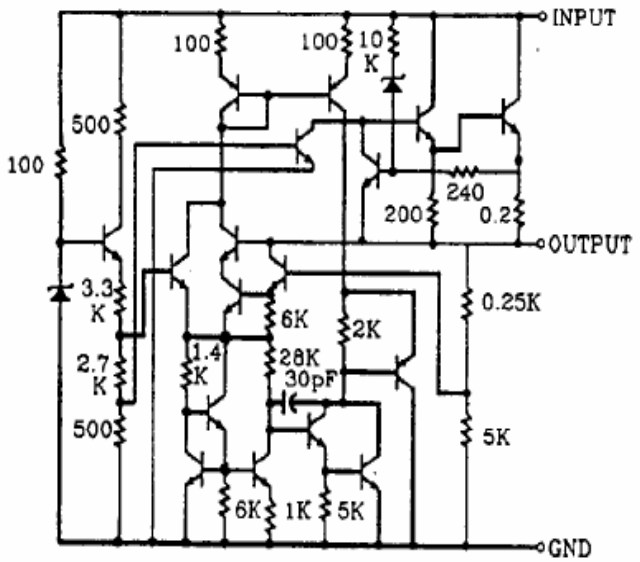
PIN ARRANGEMENT

PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2.)

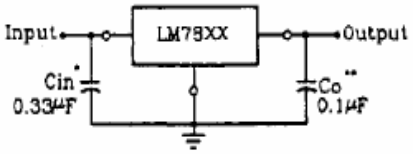
CIRCUIT SCHEMATIC

REPRESENTATIVE SCHEMATIC DIAGRAM



TYPICAL CONNECTING CIRCUIT

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0V above the output voltage even during the low point on the Input ripple voltage.

XX = these two digits of the type number indicate voltage.

* =Cin is required if regulator is located an appreciable distance from power supply filter.

** =Co is not needed for stability; however, it does improve transient response.

10.PT2314

• **Description**

PT2314 is a four-channel input digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance are incorporated into a single chip. Loudness Function and Selectable Input Gain are also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the I2C Bus. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage for audio application.

• **Features**

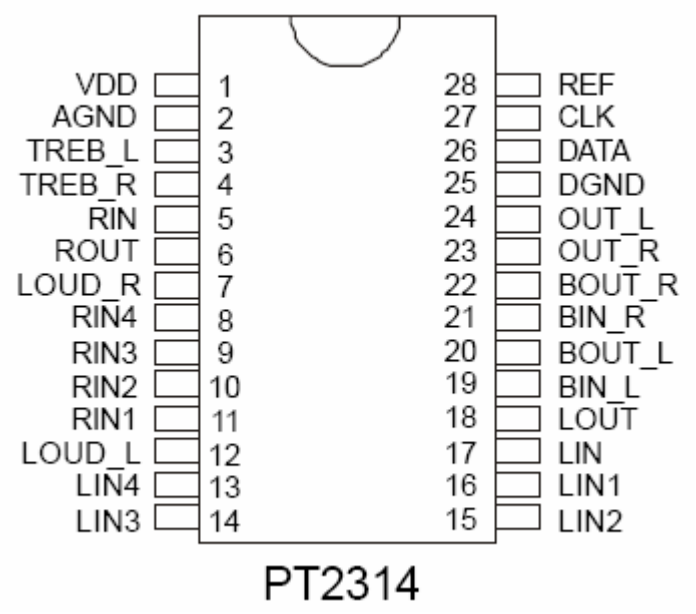
CMOS Technolog

. Least External Components
. Treble and Bass Control
. Loudness Function
. 4 Stereo Inputs with Selectable Input Gain
. Input/Output for External Noise Reduction System/Equalizer
. 2 Independent Speaker Controls for Balance Control
. Independent Mute Function
. Volume Control in 1.25 dB/step
. Low Distortion
. Low Noise and DC Stepping
. Controlled by I2C Bus Micro-Processor Interface
. Available in 28 Pins, DIP/SO Package

• **Applications**

. Car Stereo (Audio)
. Hi-Fi Audio System

• **Pin Configuration**



• **Pin Description**

Pin Name	I/O	Description	Pin No.
VDD	-	Supply Input Voltage	1
AGND	-	Analog Ground	2
TREB_L	I	Left Channel Input for Treble Controller	3
TREB_R	I	Right Channel Input for Treble Control	4
RIN	I	Audio Processor Right Channel Input	5
ROUT	O	Gain Output and Input Selector for Right Channel	6
LOUD_R	I	Right Channel Loudness Input	7
RIN4	I	Right Channel Input 4	8
RIN3	I	Right Channel Input 3	9
RIN2	I	Right Channel Input 2	10
RIN1	I	Right Channel Input 1	11
LOUD_L	I	Left Channel Loudness Input	12
LIN4	I	Left Channel Input 4	13
LIN3	I	Left Channel Input 3	14
LIN2	I	Left Channel Input 2	15
LIN1	I	Left Channel Input 1	16
LIN	I	Audio Processor Left Channel Input	17
LOUT	O	Gain Output and Input Selector for Left Channel	18
BIN_L	I	Left Channel Input for Bass Controller	19
BOUT_L	O	Left Bass Controller Output Channel	20
BIN_R	I	Right Channel Input for Bass Controller	21
BOUT_R	O	Right Channel Output for Bass Controller	22
OUT_R	O	Right Speaker Output	23
OUT_L	O	Left Speaker Output	24
DGND	-	Digital Ground	25
DATA	I	Control Data Input	26
CLK	I	Clock Input for Serial Data Transmission	27
REF	-	Analog Reference Voltage (1/2 VDD)	28

11.TDA1517P **2 x 6 W stereo power amplifier**

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin (SIL9MPF), a plastic rectangular-bent single in-line medium power package with fin (RBS9MPF) or a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for multi-media applications.

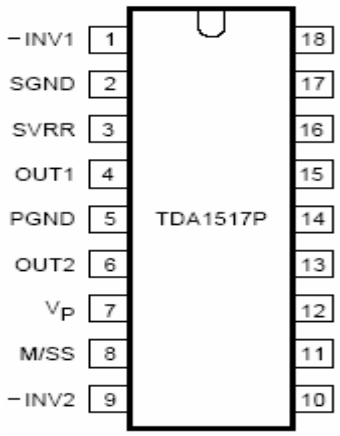
- **Features**

Requires very few external components
High output power
Fixed gain
Good ripple rejection
Mute/standby switch
AC and DC short-circuit safe to ground and VP
Thermally protected
Reverse polarity safe
Capability to handle high energy on outputs (VP = 0 V)
No switch-on/switch-off plop
Electrostatic discharge protection

- **Pin Description**

SYMBOL	PIN	DESCRIPTION
-INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
VP	7	supply voltage
M/SS	8	mute/standby switch input
-INV2	9	non-inverting input 2

- **Pin Configuration**



- **DC Characteristics**

VP = 14.4 V; Tamb = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
V_O	DC output voltage		–	6.95	–	V
Mute/standby switch						
V_8	switch-on voltage level	see Fig.5	8.5	–	–	V
Mute condition						
V_O	output signal in mute position	$V_{I(max)}$ = 1 V; f_i = 20 Hz to 15 kHz	–	–	2	mV
Standby condition						
I_{sb}	DC current in standby condition		–	–	100	µA
V_{sw}	switch-on current		–	12	40	µA

Note

The circuit is DC adjusted at VP = 6 to 18 V and AC operating at VP = 8.5 to 18 V.

ICS ON DVD BOARD

1.AP1513 (See Page 13)

2.LM1117 (See Page 14)

3.MT1389HD

Abbr. :
SR : Slew Rate
PU : Pull Up
PD : Pull Down
SMT : Schmitt Trigger
2MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (26)				
231	RFGND18		Ground	Analog ground
232	RFVDD18		Power	Analog power 1.8V
252	OSP		Analog output	RF Offset cancellation capacitor connecting
253	OSN		Analog output	RF Offset cancellation capacitor connecting
254	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input

ALPC (4)				
Pin	**Main**	**Alt.**	**Type**	**Description**
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
ADC Power (2)				
244	ADCVDD3		Power	Analog 3.3V Power for ADC
245	ADCVSS		Ground	Analog ground for ADC
VPLL (3)				
43	VPLLVSS		Ground	Analog ground for VPLL
44	CAPPAD		Analog Inout	VPLL External Capacitance connection
45	VPLLVDD3		Power	Analog 3.3V Power for VPLL
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) 2) Central servo Positive main beam summing output
26	RFLVL	RFON	Analog output	1) 2) RFRP low pass, or Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (6)				
246	RFVDD3		Power	Analog Power
247	RFRPDC		Analog output	RF ripple detect output
248	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
249	HRFZC		Analog Input	High frequency RF ripple zero crossing
250	CRTPLP		Analog output	Defect level filter capacitor connecting
251	RFGND		Ground	Analog Power

RF Data PLL Interface (9)				
Pin	**Main**	**Alt.**	**Type**	**Description**
235	JITFO		Analog output	The output terminal of RF jitter meter.
236	JITFN		Analog Input	The input terminal of RF jitter meter.
237	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.
238	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
239	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
240	LPFON		Analog Output	The negative output of loop filter amplifier
241	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
242	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
243	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENP W M		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT 1	V_ADIN9	Analog Output	1) 1st General PWM output, or 2) Version AD input 9
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
50	FG (Diogital pin)	V_ADIN8	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for V_ADIN8	1) Motor Hall sensor input, or 2) Version AD input 8
General Power/Ground (18)				
55,93, 142,160, 174, 213	DVDD18		Power	1.8V power pin for internal digital circuitry
81,178	DVSS		Ground	1.8V Ground pin for internal digital circuitry
65,96,118, 131,145, 156, 170, 208	DVDD3		Power	3.3V power pin for internal digital circuitry
90, 148	DVSS		Ground	3.3V Ground pin for internal digital circuitry

Micro Controller and Flash Interface (48)				
Pin	**Main**	**Alt.**	**Type**	**Description**
62	HIGHA0		Inout 2~16MA, SR PU	Microcontroller address 8
74	HIGHA1		Inout 2~16MA, SR PU	Microcontroller address 9
73	HIGHA2		Inout 2~16MA, SR PU	Microcontroller address 10
72	HIGHA3		Inout 2~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Inout 2~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Inout 2~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Inout 2~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Inout 2~16MA, SR PU	Microcontroller address 15
89	AD7		Inout 2~16MA, SR	Microcontroller address/data 7
86	AD6		Inout 2~16MA, SR	Microcontroller address/data 6
85	AD5		Inout 2~16MA, SR	Microcontroller address/data 5
84	AD4		Inout 2~16MA, SR	Microcontroller address/data 4
83	AD3		Inout 2~16MA, SR	Microcontroller address/data 3
82	AD2		Inout 2~16MA, SR	Microcontroller address/data 2
80	AD1		Inout 2~16MA, SR	Microcontroller address/data 1
79	AD0		Inout 2~16MA, SR	Microcontroller address/data 0
92	IOA0		Inout 2~16MA, SR PU	Microcontroller address 0 / IO

Pin	Main	Alt.	Type	Description
77	IOA1		Inout 2~16MA, SR PU	Microcontroller address 1 / IO
56	IOA2		Inout 2~16MA, SR PU	Microcontroller address 2 / IO
57	IOA3		Inout 2~16MA, SR PU	Microcontroller address 3 / IO
58	IOA4		Inout 2~16MA, SR PU	Microcontroller address 4 / IO
59	IOA5		Inout 2~16MA, SR PU	Microcontroller address 5 / IO
60	IOA6		Inout 2~16MA, SR PU	Microcontroller address 6 / IO
61	IOA7		Inout 2~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Output 2~16MA, SR	Flash address 16
91	A17		Output 2~16MA, SR	Flash address 17
63	IOA18		Inout 2~16MA, SR SMT	Flash address 18 / IO
64	IOA19		Inout 2~16MA, SR SMT	Flash address 19 / IO
75	IOA20		Inout 2~16MA, SR SMT	Flash address 20 / IO
87	IOA21		Inout 2~16MA, SR SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: I) GPIO
88	ALE		Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable

Pin	Main	Alt.	Type	Description
78	IOOE#		Inout 2~16MA, SR SMT	Flash output enable, active low / IO
66	IOWR#		Inout 2~16MA, SR SMT	Flash write enable, active low / IO
76	IOCS#		Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO
94	UWR#		Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
95	URD#		Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
97	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
98	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
99	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
100	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
101	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
102	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
103	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
104	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
105	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin

106	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
109	IR		Input SMT	IR control signal input
110	INTO#		Inout 4MA, SR PU, SMT	Microcontroller external interrupt 0, active low

Audio interface (28)

Pin	Main	Alt.	Type	Description
204	SPMCLK	SCLK0	Inout Non-pull	1) Audio DAC master clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 clock pin II) GPIO
205	SPDATA	SDIN0	Inout Non-pull	1) Audio data of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-in II) GPIO
206	SPLRCK	SDO0	Inout Non-pull	1) Audio left/right channel clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-out II) GPIO
207	SPBCK	SDCS0 ASDATA5	Inout Non-pull	1) Audio bit clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 chip select II) Audio serial data 5 part I : DSD data sub-woofer channel or Microphone output III) GPIO
209	ALRCK		Inout 4MA, PD, SMT	1) Audio left/right channel clock Trap value in power-on 2) reset: I) 1 : use external 373 II) 0: use internal 373
210	ABCK	Fs64	Output 4MA Non-pull	1) Audio bit clock 2) Phase de-modulation
211	ACLK		Inout 4MA Non-pull	Audio DAC master clock

197	ASDATA0		Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) DSD data left channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While using external channels: I) GPO_2
202	ASDATA1		Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) DSD data right channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While using external channels: I) GPO_1
203	ASDATA2		Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) DSD data left surround 2) channel Trap value in power-on reset : I) 1 : manufactory 3) test mode II) 0 : normal operation While using external 4) channels: I) GPO_0
212	ASDATA3		Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) DSD data right surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPO_0
214	ASDATA4	INT1#	Inout 4MA PD SMT	1) Audio serial data 4 (Down-mixed Left/Right) 2) DSD data center channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) Microcontroller external interrupt 1 II) GPO_0
215	MC_DATA	INT2#	Inout PD SMT	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPO_0
216	SPDIF		Output 2~16MA, SR : ON/OFF Non-pull	SPDIF output

217	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
218	APLLCAP		Analog Inout	APLL External Capacitance connection
219	APLLVSS		Ground	Ground pin for audio clock circuitry
220	ADACVSS2		Ground	Ground pin for AUDIO DAC circuitry
221	ADACVSS1		Ground	Ground pin for AUDIO DAC circuitry
222	ARF	GPIO	Output	1) AUDIO DAC Sub-woofer channel output While internal 2) AUDIO DAC not used: GPIO
223	ARS	GPIO	Output	1) AUDIO DAC Right Surround channel output 2) While internal AUDIO DAC not used: a. SDATA3 b. GPIO
224	AR	GPIO	Output	1) AUDIO DAC Right channel output 2) While internal AUDIO DAC not used: a. SDATA1 b. GPIO
225	AVCM		Analog	AUDIO DAC reference voltage
226	AL	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA2 b. GPIO
227	ALS	GPIO	Output	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. SDATA0 b. GPIO
228	ALF	GPIO	Output	1) AUDIO DAC Center channel output 2) While internal AUDIO DAC not used:GPIO
229	ADACVDD1		Power	3.3V power pin for AUDIO DAC circuitry
230	ADACVDD2		Power	3.3V power pin for AUDIO DAC circuitry

Video Interface (18)				
196	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
195	VREF		Analog	Bandgap reference voltage
194	FS		Analog	Full scale adjustment
193	YUV0	CIN	Output 4MA, SR	1) Video data output bit 0 2) Compensation capacitor
192	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
191	YUV1	Y	Output 4MA, SR	1) Video data output bit 1 2) Analog Y output
190	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
189	YUV2	C	Output 4MA, SR	1) Video data output bit 2 2) Analog chroma output
188	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
187	YUV3	CVBS	Output 4MA, SR	1) Video data output bit 3 2) Analog composite output

186	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
185	YUV4	Y/G	Output 4MA, SR	1) Video data output bit 4 2) Green or Y
184	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
183	YUV5	B/Cb/Pb	Output 4MA, SR	1) Video data output bit 5 2) Blue or CB
182	YUV6	R/Cr/Pr	Output 4MA, SR	1) Video data output bit 6 2) Red or CR
181	VSYN	V_ADIN1	Inout 4MA, SR SMT Non-pull	1) Vertical sync input/output 2) While no External TV-encoder: I) Vertical sync for video-input II) Version AD input port 1 III) GPIO
180	YUV7	INT3# ASDATA5	Inout 4MA, SR SMT Non-pull	1) Video data output bit 7 2) While no External TV-encoder: I) Microcontroller external interrupt 3 II) Audio serial data 5 part II : DSD data sub-woofer channel or Microphone output III) GPIO
179	HSYN	INT4# V_ADIN2	Inout 4MA, SR SMT Non-pull	1) Horizontal sync input/output 2) While no External TV-encoder: I) Horizontal sync for video-input II) Microcontroller external interrupt 4 III) Version AD input port 2 IV) GPIO
MISC (12)				
46	USB_VSS		USB Ground	USB ground pin
47	USBP		Analog Inout	USB port DPLUS analog pin
48	USBM		Analog Inout	USB port DMINUS analog pin
49	USB_VDD3		USB Power	USB Power pin 3.3V
108	PRST#		Input PU, SMT	Power on reset input, active low
107	ICE		Input PD, SMT	Microcontroller ICE mode enable
233	XTALO		Output	27M crystal out
234	XTALI		Input	27M crystal in
201	GPIO_3		Inout Pull-Down	GPIO
200	GPIO_4		Inout Pull-Down	GPIO
199	RCLKB	GPIO_5	Inout Pull-Up	GPIO
198	RVREF	GPIO_6	Inout Pull-Up	GPIO

Dram Interface (58) (Sorted by position)				
176	C_0	IO_0 (RD16)	Inout Non-pull	1) Digital Video output C bit 0 2) GPIO
175	C_1	IO_1 (RD17)	Inout Non-pull	1) Digital Video output C bit 1 2) GPIO
173	C_2	IO_2 (RD18)	Inout Non-pull	1) Digital Video output C bit 2 2) GPIO
172	C_3	IO_3 (RD19)	Inout Non-pull	1) Digital Video output C bit 3 2) GPIO
171	C_4	IO_4 (RD20)	Inout Non-pull	1) Digital Video output C bit 4 2) GPIO
169	C_5	IO_5 (RD21)	Inout Non-pull	1) Digital Video output C bit 5 2) GPIO
168	C_6	IO_6 (RD22)	Inout Non-pull	1) Digital Video output C bit 6 2) GPIO
167	C_7	IO_7 (RD23)	Inout Non-pull	1) Digital Video output C bit 7 2) GPIO

177	IO_17	(DQM2)	Inout Non-pull	GPIO
166	YUVCLK	IO_8 (DQM3)	Inout Non-pull	1) Digital Video output Clock 2) GPIO
165	Y_0	IO_9 (RD24)	Inout Non-pull	1) Digital Video output Y bit 0 2) GPIO
164	Y_1	IO_10 (RD25)	Inout Non-pull	1) Digital Video output Y bit 1 2) GPIO
163	Y_2	IO_11 (RD26)	Inout Non-pull	1) Digital Video output Y bit 2 2) GPIO
162	Y_3	IO_12 (RD27)	Inout Non-pull	1) Digital Video output Y bit 3 2) GPIO
161	Y_4	IO_13 (RD28)	Inout Non-pull	1) Digital Video output Y bit 4 2) GPIO
159	Y_5	IO_14 (RD29)	Inout Non-pull	1) Digital Video output Y bit 5 2) GPIO
158	Y_6	IO_15 (RD30)	Inout Non-pull	1) Digital Video output Y bit 6 2) GPIO
157	Y_7	IO_16 (RD31)	Inout Non-pull	1) Digital Video output Y bit 7 2) GPIO

155	RA4		Inout	DRAM address 4
154	RA5		Inout	DRAM address 5
153	RA6		Inout	DRAM address 6
152	RA7		Inout	DRAM address 7

151	RA8		Inout	DRAM address 8
150	RA9		Inout	DRAM address 9
149	RA11		Inout Pull-Down	DRAM address bit 11
147	CKE		output	DRAM clock enable
146	RCLK		Inout	Dram clock
144	RA3		Inout	DRAM address 3
143	RA2		Inout	DRAM address 2
141	RA1		Inout	DRAM address 1
140	RA0		Inout	DRAM address 0
139	RA10		Inout	DRAM address 10
138	BA1		Inout	DRAM bank address 1
137	BA0		Inout	DRAM bank address 0
136	RCS#		output	DRAM chip select, active low
135	RAS#		output	DRAM row address strobe, active low
134	CAS#		output	DRAM column address strobe, active low
133	RWE#		output	DRAM Write enable, active low
132	DQM1		Inout	Data mask 1
130	IO_18	(DQS1)	Inout Non-pull	GPIO
129	RD8		Inout	DRAM data 8
128	RD9		Inout	DRAM data 9

127	RD10		Inout	DRAM data 10
126	RD11		Inout	DRAM data 11
125	RD12		Inout	DRAM data 12
124	RD13		Inout	DRAM data 13
123	RD14		Inout	DRAM data 14
122	RD15		Inout	DRAM data 15
121	RD0		Inout	DRAM data 0
120	RD1		Inout	DRAM data 1
119	RD2		Inout	DRAM data 2
117	RD3		Inout	DRAM data 3
116	RD4		Inout	DRAM data 4
115	RD5		Inout	DRAM data 5
114	RD6		Inout	DRAM data 6
113	RD7		Inout	DRAM data 7
112	IO_19	(DQS0)	Inout Non-pull	GPIO
111	DQM0		Inout	Data mask 0

JTAG Interface(4)					
51	TDI	V_ADIN4	Inout Non-pull	1) 2) 3)	Serial interface port 3 data-out Version AD input port 4 GPIO
52	TMS	V_ADIN5	Inout Non-pull	1) 2) 3)	Serial interface port 3 data-in Version AD input port 5 GPIO
53	TCK	V_ADIN6	Inout Non-pull	1) 2) 3)	Serial interface port 3 clock pin Version AD input port 6 GPIO
54	TDO	V_ADIN7	Inout Non-pull	1) 2) 3)	Serial interface port 3 chip-select Version AD input port 7 GPO

Note:

1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The video input port and external TV encoder mode can not both use CCIR-601 mode, at least one of them should be in CCIR-656 mode.
4. Following is a summary of modified pins.
   (a) Pin 48, 49, 50, 51 are no longer for JTAG functions.
   (b) V_ADIN0 and V_ADIN3 is not available.

4.BA5494

The AM5954 is a four-channel BTL driver IC for driving the motors and actuators such as used in CD-ROM drives. Two of the channels use current feedback to minimize the current phase shift caused by the influence of loading inductance.

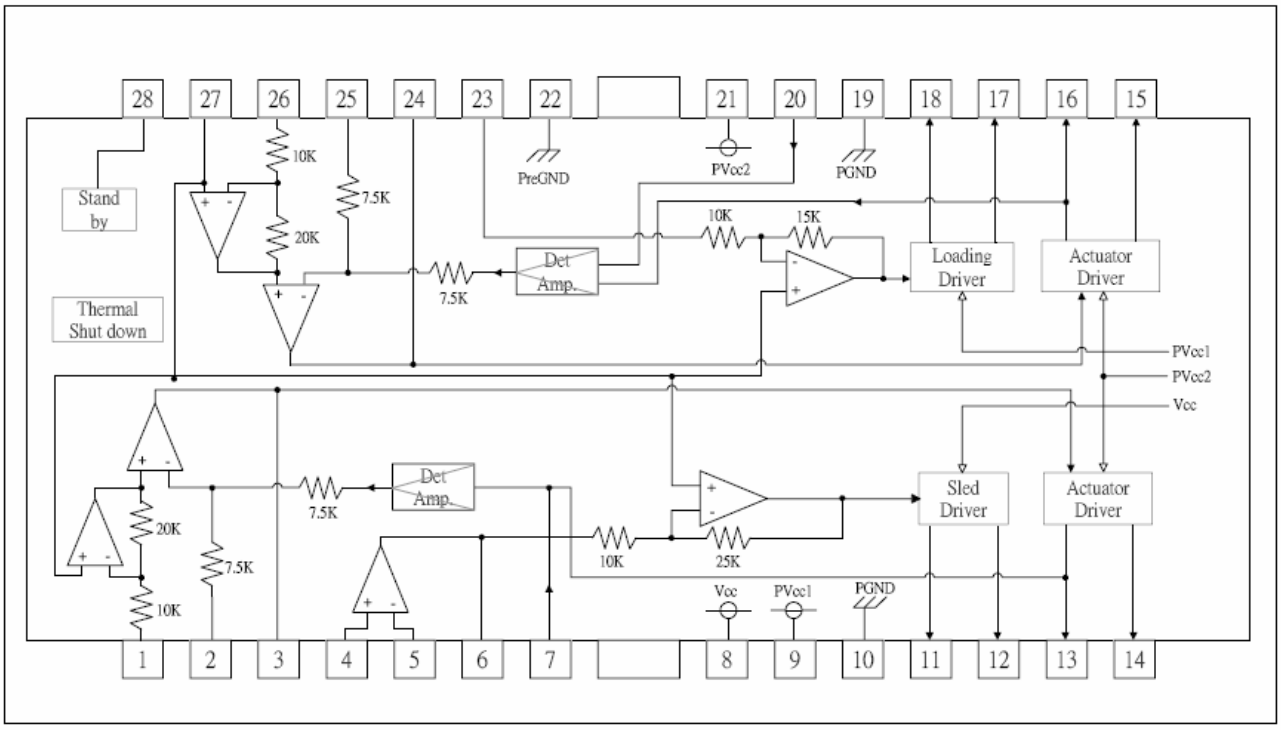
● Applications

BTL driver for CD, CD-ROM and DVD.

● Features

1) Two channels are current-type BTL drivers for actuators for tracking and focus, two channels are voltage-type BTL driver for sled and loading motors.
2) Wide dynamic range [9.0V(*typ*) when Vcc=PVcc=12V, at R_L=8Ω load].
3) Separating power of Vcc and PVcc to improve power efficiency by a low supply voltage for tracking and focus.
4) Level shift circuit built-in.
5) Thermal shut down circuit built-in.
6) Standby mode built-in.
7) **Dual actuator drivers:**
   The drivers use current feedback to minimize the current phase shift caused by the influence of the load inductance. The output structure are two power OPAMPS in bridge configuration.
8) **Sled motor driver:**
   A general purpose input OP provides differential input for signal addition. The output structure are two power OPAMPS in bridge configuration.
9) **Loading driver:**
   Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.

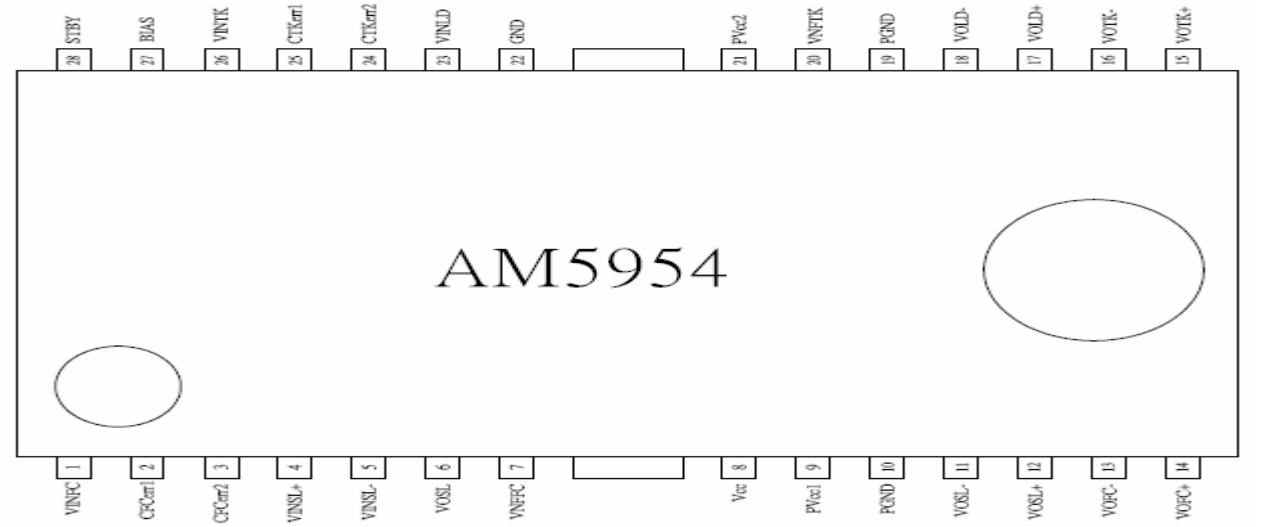
● Block diagram



● Pin description

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	CFCerr1	Connection of capacitor for the error amp filter
3	CFCerr2	Connection of capacitor for the error amp filter
4	VINSL+	OPAMP input (+) for the sled driver
5	VINSL-	OPAMP input (-) for the sled driver
6	VOSL	OPAMP output for the sled driver
7	VNFFC	Focus driver feedback pin
8	Vcc	Vcc for pre-drive block and power block of sled
9	PVcc1	Vcc for power block of loading
10	PGND	GND for power block
11	VOSL-	Sled driver output (-)
12	VOSL+	Sled driver output (+)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Loading driver output (+)
18	VOLD-	Loading driver output (-)
19	PGND	GND for power block
20	VNFTK	Feedback for tracking driver
21	PVcc2	Vcc for power block of tracking and focus
22	GND	GND for pre-drive block
23	VINLD	Input for loading driver
24	CTKerr2	Connection of capacitor for the error amp filter
25	CTKerr1	Connection of capacitor for the error amp filter
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	STBY	Input for standby control

● Pin configuration



5.BA6208F

The BA6208F is monolithic ICs used for driving reversible motors. It allows control of reversible motors in cassette players and other electrical equipment by using TTL-level logic signals. The IC contains a logic section, which controls forward and reverse rotations as well as forced stop, and an output power section, which can supply an output current of up to 100mA (typical) according to the logic control.

●Features

1) Motor driving power transistors are built in (100mA typically).
2) Brake is applied when stopping the motor (when inputs A and B are both HIGH level).
3) Built-in diode to absorb surge currents.
4) Very low standby circuit current when inputs A and B are both LOW level.
5) Wide range of operating supply voltage (4.5 ~ 15.0V).
6) Direct control with the TTL logic.

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	18	V
Power dissipation	BA6208	Pd	700*1	mW
	BA6208F	Pd	450*2	
Operating temperature		Topr	−20~+60	℃
Storage temperature		Tstg	−55~+125	℃
Maximum output current		I_{OUT}	500	mA

*1 Reduced by 7 mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 4.5 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	—	15	V

●Input truth table

3pin (Ain)	2pin (Bin)	8pin (Aout)	7pin (Bout)
H	L	H	L
L	H	L	H
H	H	L	L
L	L	OPEN	OPEN

Note : HIGH level input is 2.0 V or more.
LOW level input is 0.8 V or less.

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{CC} = 9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output current	I_O	200	—	—	mA	
Output saturation voltage	V_{CE}	—	—	1.6	V	I_O=100mA
Input high level voltage	V_{IH}	2.0	—	—	V	
Input low level voltage	V_{IL}	—	—	0.8	V	
Standby supply current	I_{ST}	—	—	0.4	mA	When inputs A and B are both LOW level
Input high level current	I_{IH}	—	—	400	μA	V_{IH}=4.5V

A diode that absorbs at least 500 mA is built in to give protection against surge currents with a pulse width of 10 ms and a duty ratio of 10% or less.

6.K4S641632H-TC60 SDRAM 64Mb H-die(x16)

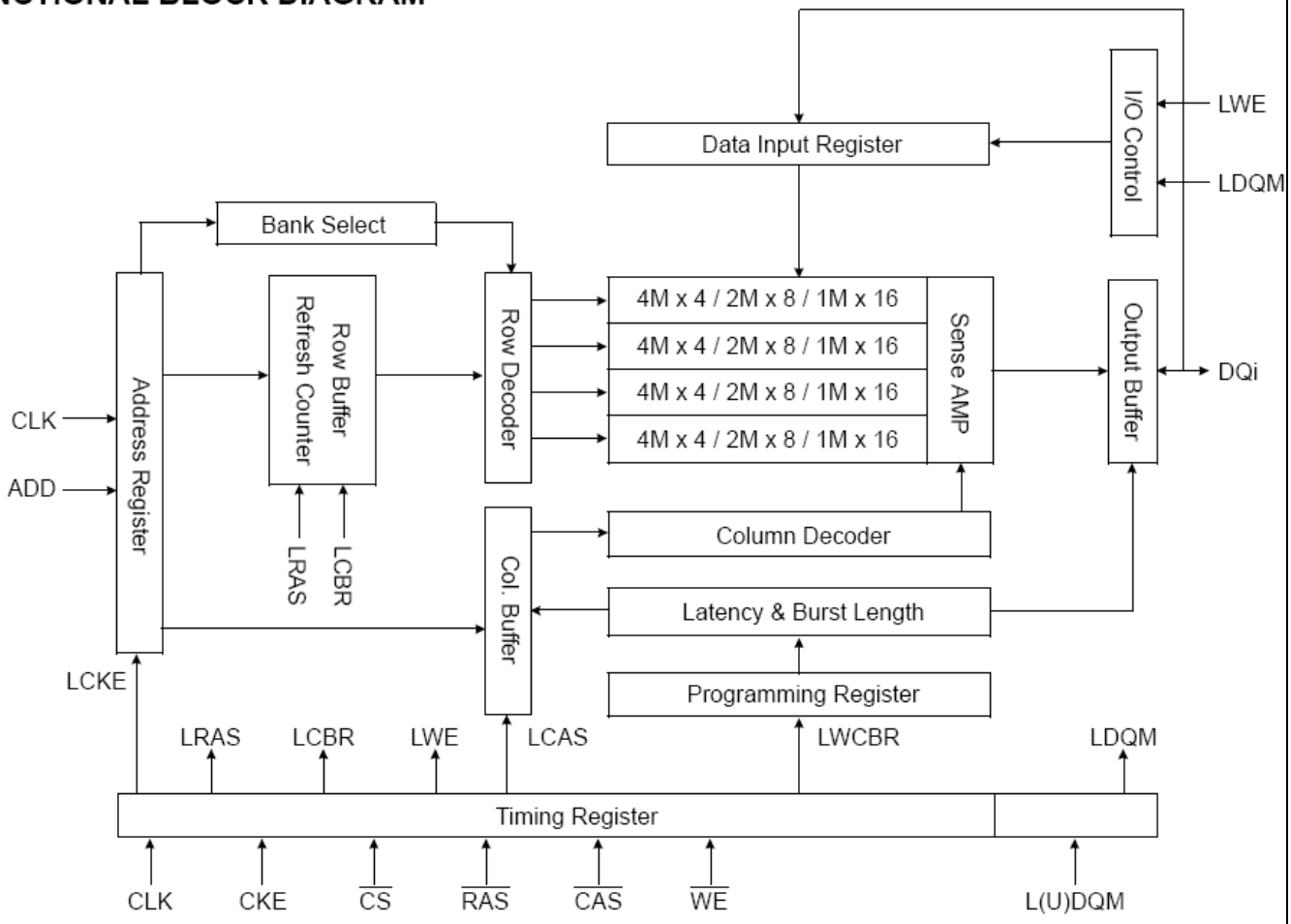
The K4S641632H is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

• **Information**

Part No.	Organization	Max Freq	Interface	Package
K4S641632H-TC(L)60	4Mb x 16	166MHz(CL=3)	LVTTL	54 pin TSOP(II)
K4S641632H-TC(L)60	4Mb x 16	166MHz(CL=3)	LVTTL	54 pin TSOP(II)

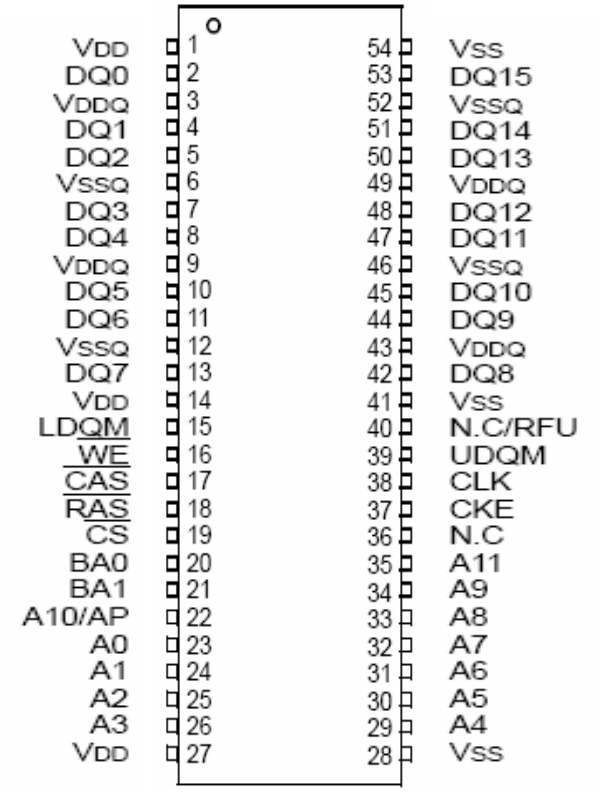
Row Address	Column Address
A0～A11	A0～A9

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

• **Pin Configuration (top view)**



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : (x4 : CA_0 ~ CA_9, x8 : CA_0 ~ CA_8, x16 : CA_0 ~ CA_7)
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ $_N$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins. (x4 : DQ_0 ~ $_3$), (x8 : DQ_0 ~ $_7$), (x16 : DQ_0 ~ $_{15}$)
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

7. MX29LV160BT

16M-BIT[2Mx8/1Mx16]CMOS SINGLE VOLTAGE 3V ONLY FLASHMEMORY

FEATURES

- Extended single - supply voltage range 2.7V to 3.6V
- 2,097,152 x 8/1,048,576 x 16 switchable
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- **Fully compatible with MX29LV160A device**
- Fast access time: 55/70ns
- Low power consumption
  - 30mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - Byte/word Programming (9us/11us typical)
  - Sector Erase (Sector structure 16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x31)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase operation completion.
- Ready/$\overline{\text{Busy}}$ pin (RY/$\overline{\text{BY}}$)
  - Provides a hardware method of detecting program or erase operation completion.
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotect allows code changes in previously locked sectors.
- CFI (Common Flash Interface) compliant
  - Flash device parameters stored on the device and provide the host system to access
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 1.4V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
  - 48-ball CSP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash

GENERAL DESCRIPTION

The MX29LV160BT/BB is a 16-mega bit Flash memory organized as 2M bytes of 8 bits or 1M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV160BT/BB is packaged in 44-pin SOP, 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV160BT/BB offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV160BT/BB has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

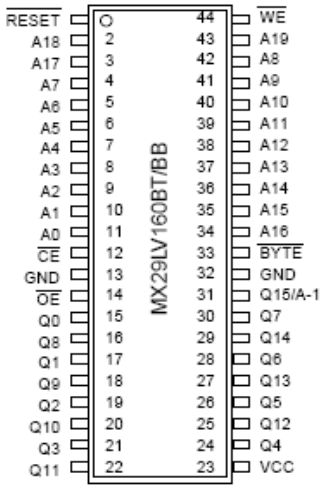
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV160BT/BB uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV160BT/BB uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

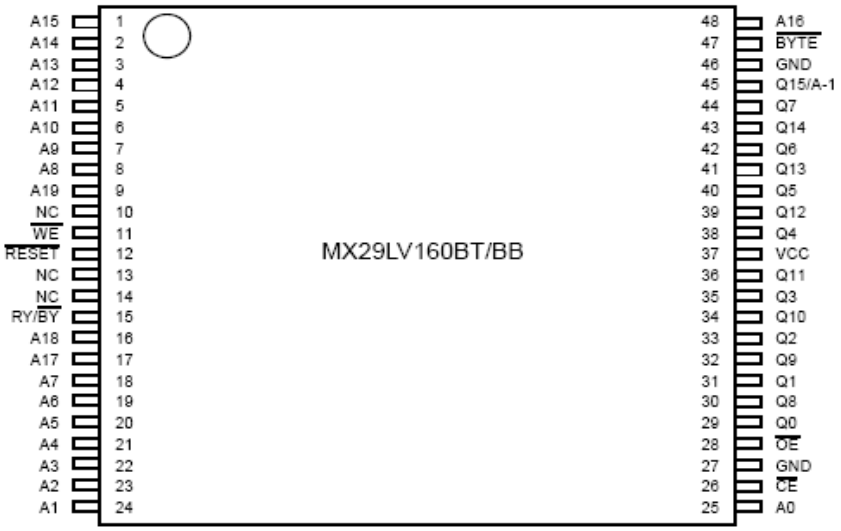
44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BYTE}$	Word/Byte Selection input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{OE}$	Output Enable Input
RY/$\overline{BY}$	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

48 TSOP (Standard Type) (12mm x 20mm)



DC CHARACTERISTICS TA = -40°C TO 85°C, VCC = 2.7V~3.6V

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS	
ILI	Input Leakage Current			± 1	uA	VIN = VSS to VCC, VCC=VCC max	
ILIT	A9 Input Leakage Current			35	uA	VCC=VCC max; A9=12.5V	
ILO	Output Leakage Current			± 1	uA	VOUT = VSS to VCC, VCC=VCC max	
ICC1	VCC Active Read Current		9	16	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	@5MHz
			2	4	mA	(Byte Mode)	@1MHz
			9	16	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	@5MHz
			2	4	mA	(Word Mode)	@1MHz
ICC2	VCC Active write Current		20	30	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH, $\overline{WE}$=VIL	
ICC3	VCC Standby Current		0.2	5	uA	$\overline{CE}$; $\overline{RESET}$=VCC ± 0.3V	
ICC4	VCC Standby Current During Reset (See Conditions)		0.2	5	uA	$\overline{RESET}$=VSS ± 0.3V	
ICC5	Automatic sleep mode		0.2	5	uA	VIH=VCC ± 0.3V;VIL=VSS ± 0.3V	
VIL	Input Low Voltage (Note 1)	-0.5		0.8	V		
VIH	Input High Voltage	0.7xVCC		VCC+ 0.3	V		
VID	Voltage for Automatic Select and Temporary Sector Unprotect	11.5		12.5	V	VCC=3.3V	
VOL	Output Low Voltage			0.45	V	IOL = 4.0mA, VCC= VCC min	
VOH1	Output High Voltage (TTL)	0.85xVCC				IOH = -2mA, VCC=VCC min	
VOH2	Output High Voltage (CMOS)	VCC-0.4				IOH = -100uA, VCC min	
VLKO	Low VCC Lock-out Voltage	1.4		2.1	V		

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for tACC +30ns.

8.AT24C16

2-Wire Serial CMOS E^2PROM 16k (2048 x 8)

The AT24C16 provides 16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V(4.5V to 5.5V), 2.7V(2.7V to 5.5V) and 1.8V(1.8V to 5.5V) versions.

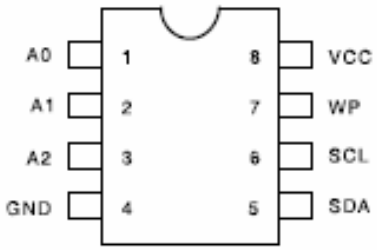
Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages

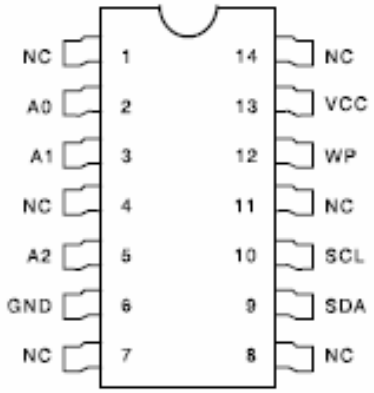
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

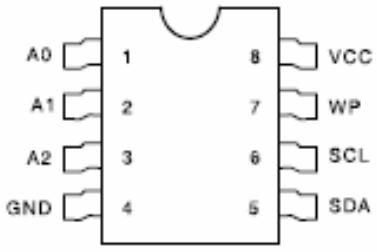
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level [1]		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level [1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time [1]		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start [1]	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time [1]		1.0		0.3	µs
t_F	Inputs Fall Time [1]		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms

Note: 1. This parameter is characterized and is not 100% tested.

9.NJM4558 DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4558/4559 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

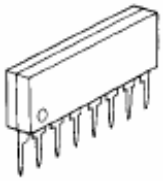
Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics.Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density.It is especially well suited for applications in differential-in,defferential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

■ PACKAGE OUTLINE

NJM4558D
NJM4559D

NJM4558M
NJM4559M

NJM4558V
NJM4559V

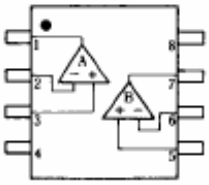


NJM4558L
NJM4559L

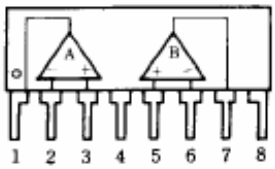
■ FEATURES

- Operating Voltage (±4V~±18V)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5MΩ typ.)
- Package Outline DIP8,DMP8,SIP8,SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM4558D,NJM4558M,NJM4558V
NJM4559D,NJM4559M,NJM4559V



NJM4558L
NJM4559L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V⁻
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V⁺

■ ELECTRICAL CHARACTERISTICS

(V^+/V^-=±15V,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	R_S≤10kΩ	-	0.5	6	mV
Input Offset Current	I_{IO}		-	5	200	nA
Input Bias Current	I_B		-	25	500	nA
Input Resistance	R_{IN}		0.3	5	-	MΩ
Large Signal Voltage Gain	A_V	R_L≥2kΩ,V_O=±10V	86	100	-	dB
Maximum Output Voltage Swing 1	V_{OM1}	R_L≥10kΩ	± 12	± 14	-	V
Maximum Output Voltage Swing 2	V_{OM2}	R_L≥2kΩ	± 10	± 13	-	V
Input Common Mode Voltage Range	V_{ICM}		± 12	14	-	V
Common Mode Rejection Ratio	CMR	R_S≤10kΩ	70	90	-	dB
Supply Voltage Rejection Ratio	SVR	R_S≤10kΩ	76.5	90	-	dB
Operating Current	I_{CC}		-	3.5	5.7	mA
Slew Rate						
NJM4558	SR		-	1	-	V/μs
NJM4559	SR		-	2	-	V/μs
Equivalent Input Noise Voltage	V_{NI}	RIAA,R_S=2.2kΩ,30kHz LPF	-	1.4	-	μVrms
Gain Bandwidth Product	GB					
NJM4558				3		MHz
NJM4559				6		MHz

10.WM8714 24-bit, 96kHz Stereo DAC

The WM8714 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8714 supports data input word lengths from 16 to 24-bits and sampling rates up to 96kHz. The WM8714 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-pin SOIC package.

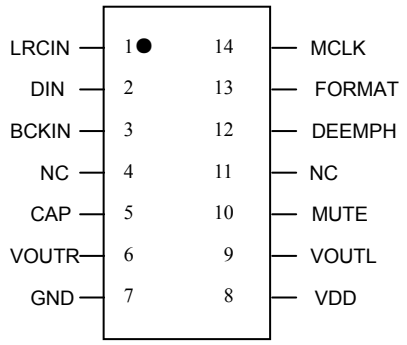
The WM8714 has a hardware control interface for selection of audio data interface format, mute and de-emphasis. The WM8714 supports I^2S, and right Justified audio data interfaces.

The WM8714 is an ideal device to interface to AC-3™, DTS ™, and MPEG audio decoders for surround sound applications, or for use in DVD players.

- **FEATURES**
  - Stereo DAC
  - Audio Performance
    - 95dB SNR ('A' weighted @ 48kHz) DAC
    - -90dB THD
  - DAC Sampling Frequency: 8kHz – 96kHz
  - Pin Selectable Audio Data Interface Format
    - I^2S, Right Justified or DSP
  - 3-5V Supply Operation
  - 14-pin SOIC Package
  - Pin Compatible with WM8725

- **APPLICATIONS**
  - DVD Players
  - Digital TV
  - Digital Set Top Boxes

- **Pin Configuration**



- **Pin Description**

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCKIN	Digital input	Bit clock input
4	NC	No connect	No internal connection
5	CAP	Analogue output	Analogue internal reference
6	VOUTR	Analogue output	Right channel DAC output
7	GND	Supply	Negative supply
8	VDD	Supply	Positive supply
9	VOUTL	Analogue output	Left channel DAC output
10	MUTE	Digital input	Soft mute control, Internal pull down High = Mute ON Low = Mute OFF
11	NC	No connect	No internal connection
12	DEEMPH	Digital input	De-emphasis select, Internal pull up High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified High = 16-24-bit I^2S
14	MCLK	Digital input	System clock input

ICS ON HI-VOLTAGE BOARD

1.BIT3193 High Performance PWM Controller

BIT3193 integrated circuit provides the essential features for general purpose PWM controller in a small low cost 16-pin package. BIT3193 has built-in a low frequency PWM generator for any specified application. BIT3193 includes latched off protection feature may make the system more reliable while compare to other similar products.

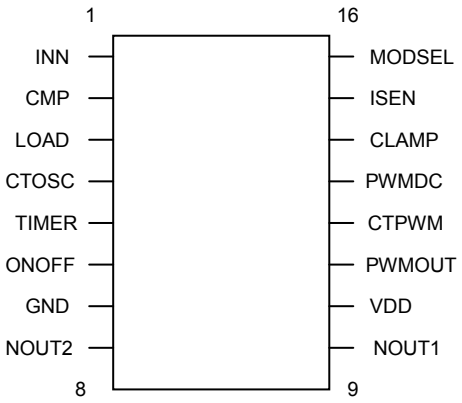
- **Features**
  - 4.5V ～ 8V operation
  - Fixed High Frequency, Voltage Mode PWM Control
  - Latched Off Protection
  - Build-In Low Frequency PWM Generator
  - Build-in UVLO
  - Low Power CMOS Process
  - Totem Pole Output
  - 16 Pin Package

- **Applications**
  - DC/DC Converters
  - LCD TV
  - LCD Monitor
  - Notebook Computer
  - Tablet PC
  - Personal Digital Assistants
  - Navigation Phone/ Door Phone
  - Portable consumer product

- **Recommended Operating Condition:**

Supply Voltage	4.5～8V
Operating Ambient Temperature	0～70 ° C
Operating Frequency	50K～400K Hz

- **Pin Layout:**



• **Pin Description**

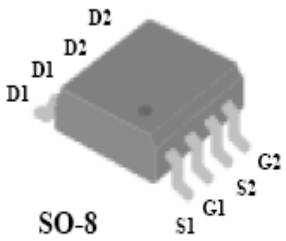
Pin No.	Symbol	I/O	Descriptions
1	INN	I/O	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	LOAD	I/O	A switch that connected to the high frequency triangle wave generator. This switch is open while ISEN pin <1.3V. An external resistor connected here may change the operation frequency of CTOSC in open load situation.
4	CTOSC	I/O	An external capacitor connected here can set the frequency of high frequency PWM controller.
5	TIMER	I/O	With internal reference current and an external capacitor connected here can set the required period of starting and the timing of initialization. The controller is forced to reset mode while TIMER<0.3V. During reset mode, a～60uA current will flow into the INN pin to reduce the output level of the error amplifier CMP to turn off the controller. The latched off protection function will be enable after this node is charged to>2.5V. System is latched off if any abnormal operation is detected if pin TIMER>2.5V. The output current of this pin is 20uA when TIMER<0.3V. The output current becomes to 1uA when TIMER>0.3V.
6	ONOFF	I	The control pin of turning on or off the IC.1V threshold with an internal 80K ±15% ohm pull-low resistor.
7	GND	I/O	The ground pin of the device.
8	NOUT2	O	The number 2 output driver for driving the NMOSFET switch.
9	NOUT1	O	The number 1 output driver for driving the NMOSFET switch.
10	VDD	I	The power supplies pin of the device.
11	PWMOUT	O	The output pin of low frequency PWM generator. A 2.5V or floating two state output is provided through this pin. The internal circuit limits the max. Duty-cycle to ～92%.
12	CTPWM	I/O	With the internal reference current and an external capacitor connected here can set the operation frequency of low frequency PWM generator with 1.0V～2.5V triangle wave output.
13	PWMDC	I	Low frequency PWM controlling input. A PWM output comes out by comparing this DC input and the 1.0～2.5V triangle wave that is generated by CTPWM.
14	CLAMP	I	Over voltage clamping. If a>2.0V voltage is detected. A～60uA current will flow into the INN pin to reduce the output of the error amplifier pin CMP to regulate the output voltage.
15	ISEN	I	Load current detection pin, the open load situation is detected if a less than 1.3V input is sensed.
16	MODSEL	O	To set the output polarity of the low frequency PWM controller.

2.AP4511M N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

▼ **Simple Drive Requirement**

▼ **Low On-resistance**

▼ **Fast Switching Performance**

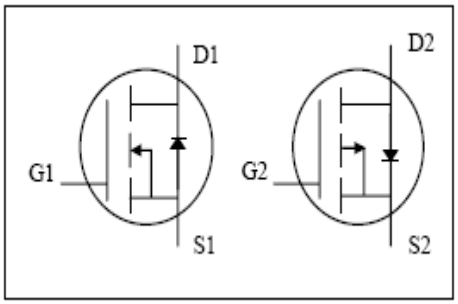


N-CH	BV_{DSS}	35V
	$R_{DS(ON)}$	25mΩ
	I_D	7A
P-CH	BV_{DSS}	-35V
	$R_{DS(ON)}$	40mΩ
	I_D	-6.1A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	35	-35	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current[3]	7	-6.1	A
I_D@T_A=70℃	Continuous Drain Current[3]	5.7	-5	A
I_{DM}	Pulsed Drain Current[1]	30	-30	A
P_D@T_A=25℃	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

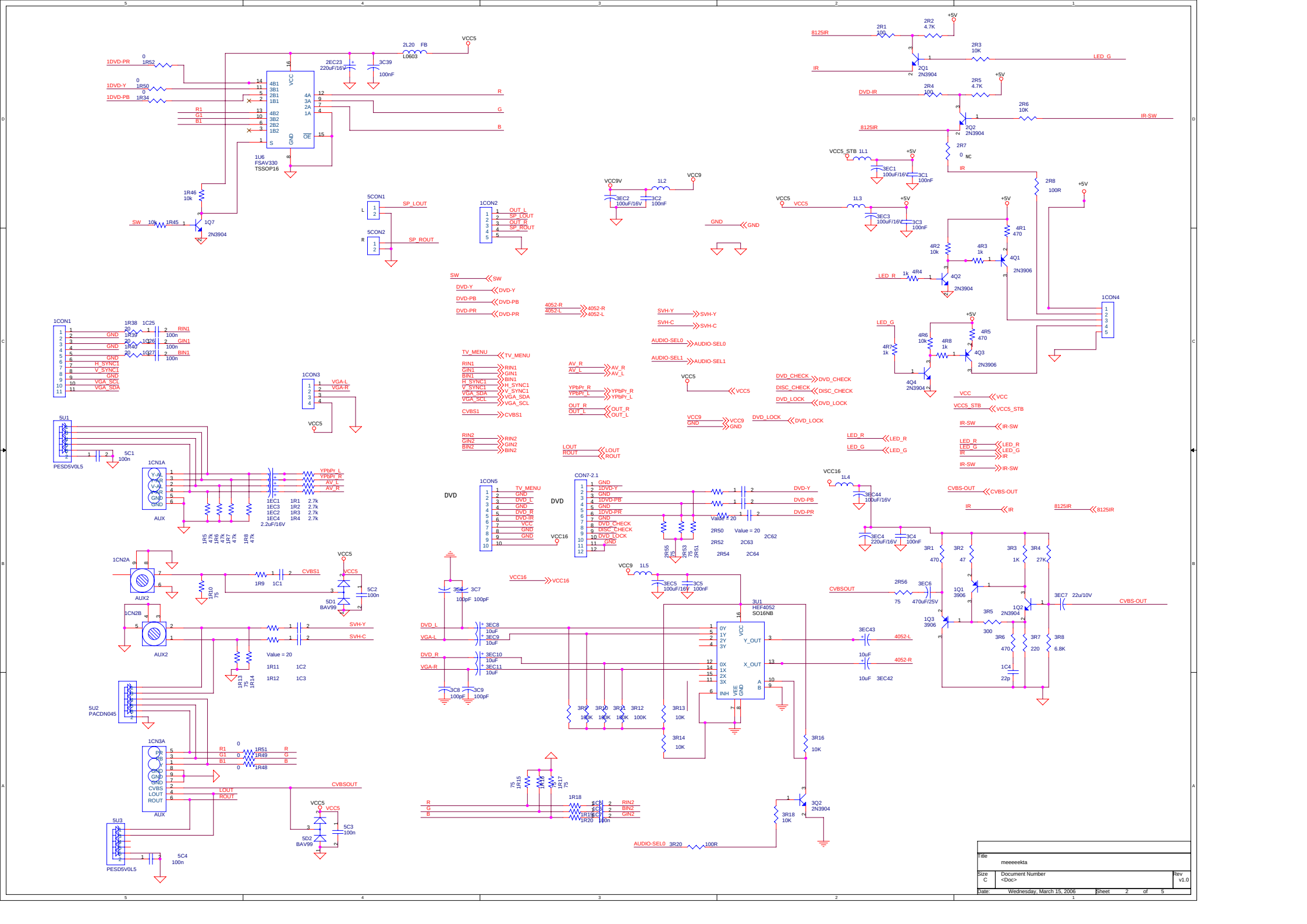
Symbol	Parameter		Value	Unit
Rthj-a	Thermal Resistance Junction-ambient[3]	Max.	62.5	℃/W

Part 3 Detailed Circuit

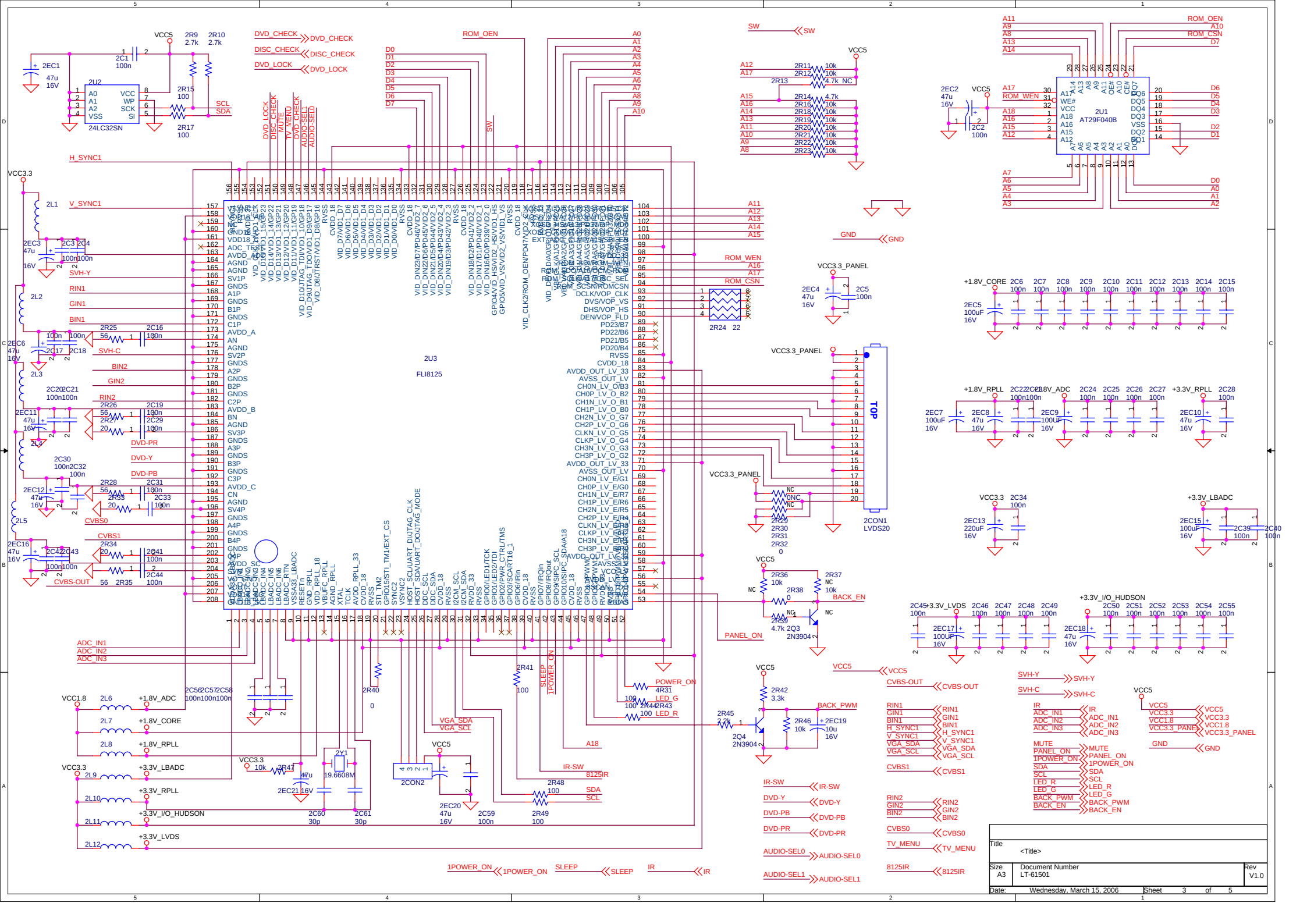
MAIN BOARD

DVD BOARD

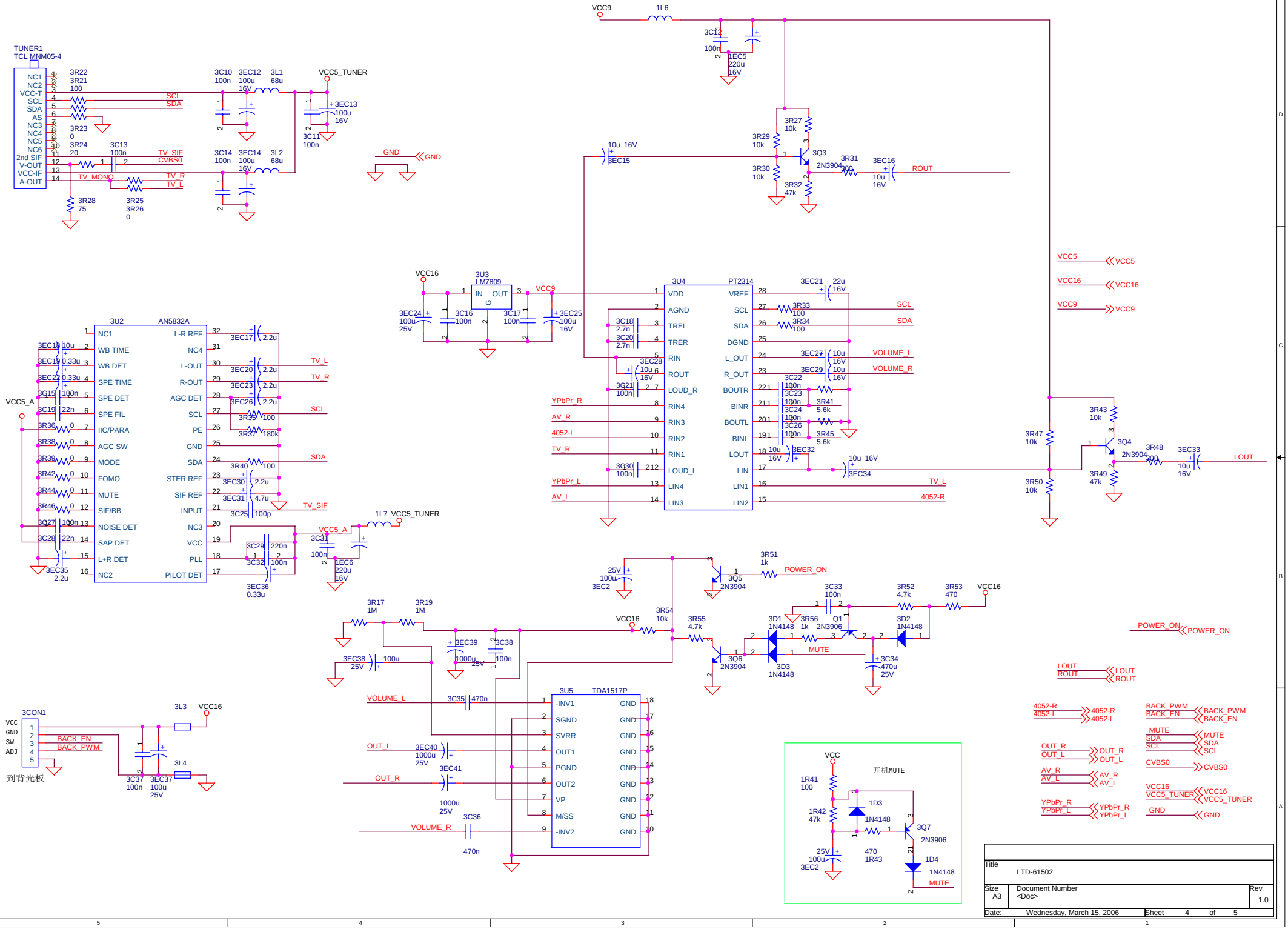
HI-VOLTAGE BOAD



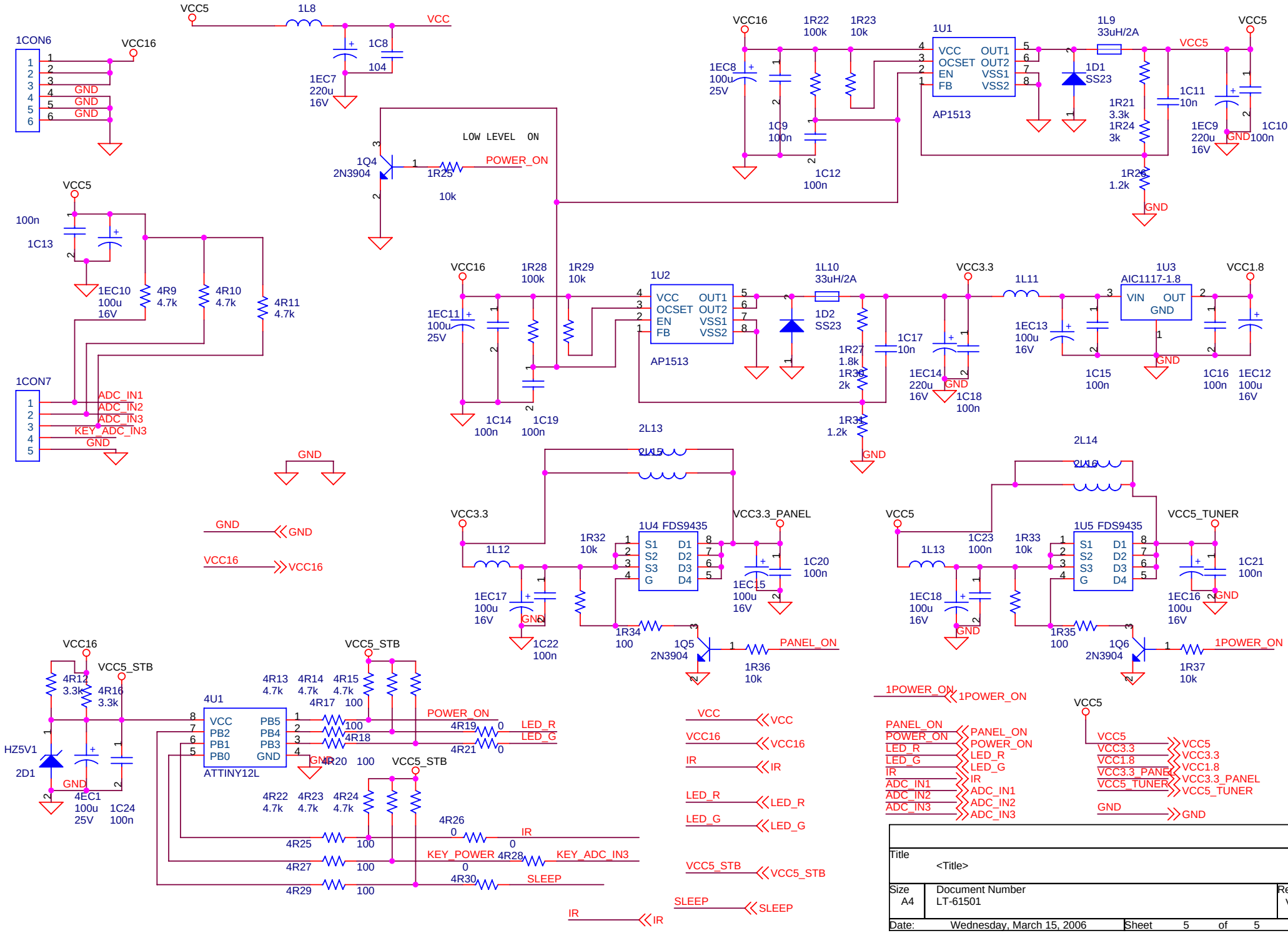
Title	meeeeekta	
Size C	Document Number <Doc>	Rev v1.0
Date: Wednesday, March 15, 2006	Sheet 2 of 5	



Title	<Title>
Size	A3
Document Number	LT-61501
Rev	V1.0
Date:	Wednesday, March 15, 2006
Sheet	3 of 5



Title	LTD-61502	
Size A3	Document Number <Doc>	Rev 1.0
Date: Wednesday, March 15, 2006	Sheet 4 of 5	


1CON6
VCC16
GND
GND
GND
VCC5
1L8
VCC
1C8
104
1EC7
220u
16V
LOW LEVEL ON
1Q4
2N3904
1R25
10k
POWER_ON
VCC16
1R22
100k
1R23
10k
1U1
VCC
OCSET
EN
FB
OUT1
OUT2
VSS1
VSS2
AP1513
1EC8
100u
25V
1C9
100n
1C12
100n
1L9
33uH/2A
VCC5
1D1
SS23
1R21
3.3k
1R24
3k
1C11
10n
1EC9
220u
16V
GND
1C10
100n
1R26
1.2k
GND
VCC5
100n
1C13
1EC10
100u
16V
4R9
4.7k
4R10
4.7k
4R11
4.7k
1CON7
ADC_IN1
ADC_IN2
ADC_IN3
KEY_ADC_IN3
GND
GND
GND
VCC16
VCC16
VCC16
1R28
100k
1R29
10k
1U2
VCC
OCSET
EN
FB
OUT1
OUT2
VSS1
VSS2
AP1513
1EC11
100u
25V
1C14
100n
1C19
100n
1L10
33uH/2A
1D2
SS23
1R27
1.8k
1R30
2k
1R31
1.2k
GND
VCC3.3
1C17
10n
1EC14
220u
16V
GND
1C18
100n
1L11
1U3
AIC1117-1.8
VIN
OUT
GND
VCC1.8
1EC13
100u
16V
1C15
100n
GND
1C16
100n
1EC12
100u
16V
2L13
2L15
VCC3.3
1L12
1R32
10k
1U4 FDS9435
S1
S2
S3
G
D1
D2
D3
D4
VCC3.3_PANEL
1C20
100n
1EC15
100u
16V
1EC17
100u
16V
GND
1C22
100n
1R34
100
1Q5
2N3904
PANEL_ON
1R36
10k
2L14
2L16
VCC5
1L13
1C23
100n
1R33
10k
1U5 FDS9435
VCC5_TUNER
1C21
100n
1EC18
100u
16V
GND
1EC16
100u
16V
GND
1R35
100
1Q6
2N3904
1POWER_ON
1R37
10k
VCC16
VCC5_STB
4R12
3.3k
4R16
3.3k
HZ5V1
2D1
GND
4EC1
100u
25V
1C24
100n
4U1
VCC
PB2
PB1
PB0
PB5
PB4
PB3
GND
ATTINY12L
4R13
4.7k
4R14
4.7k
4R15
4.7k
4R17
100
POWER_ON
4R19
0
LED_R
LED_G
4R18
4R21
0
GND
4R20
100
VCC5_STB
4R22
4.7k
4R23
4.7k
4R24
4.7k
4R26
0
IR
4R25
100
KEY_POWER
4R28
0
KEY_ADC_IN3
4R27
100
4R30
0
SLEEP
4R29
100
VCC
VCC16
IR
LED_R
LED_G
VCC5_STB
SLEEP
IR
1POWER_ON
1POWER_ON
PANEL_ON
POWER_ON
LED_R
LED_G
IR
ADC_IN1
ADC_IN2
ADC_IN3
PANEL_ON
POWER_ON
LED_R
LED_G
IR
ADC_IN1
ADC_IN2
ADC_IN3
VCC5
VCC5
VCC3.3
VCC1.8
VCC3.3_PANEL
VCC5_TUNER
GND
VCC5
VCC3.3
VCC1.8
VCC3.3_PANEL
VCC5_TUNER
GND
Title
<Title>
Size
A4
Document Number
LT-61501
Rev
V1.0
Date:
Wednesday, March 15, 2006
Sheet
5
of
5

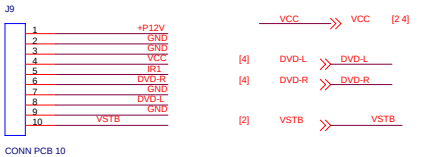
SLOTIN1389HD_TOHEI_HD62_V1

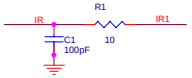
MT1389HD(LQFP256) DVD MP Board for SANYO HD62 PUH (Small Size)

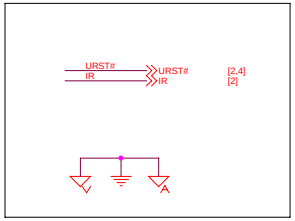
MDxxx

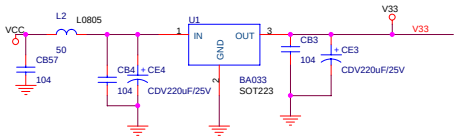
Rev	History	P#	Date
V1	The original released. (modified from 3-SY1389P3-V1) Supports 1389HD & Memory Card Interface		2005/10/08

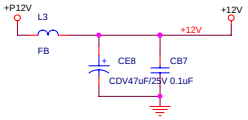
NAME	TYPE	DEVICE
VCC	Digital 5V	SUPPLY
DV33	Digital 3.3V	MT1389HD
RFV33	Servo 3.3V	MT1389HD
AV33	Laser Diode 3.3V	
V18	Digital 1.8V	MT1389HD
SD33	Digital 3.3V	SDRAM
+12V	Audio +12V	OP AMP.
-12V	Audio -12V	OP AMP.
AVDD5	Audio 5V	Audio DAC
DVDD3	Audio 3.3V	Audio DAC

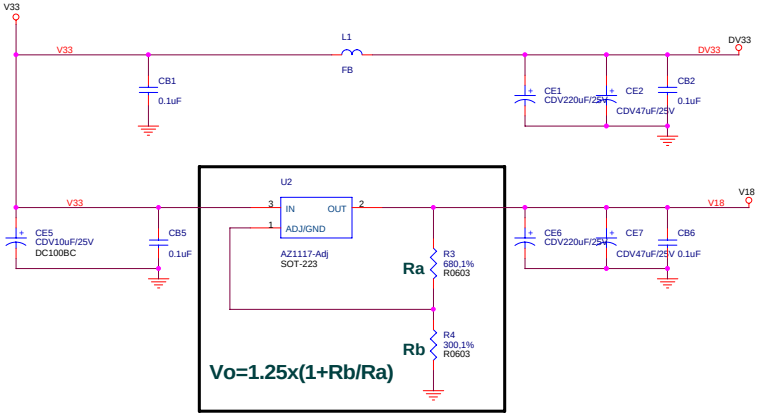


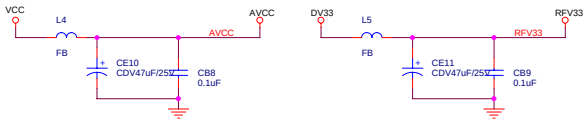


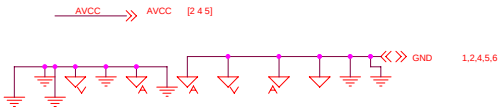




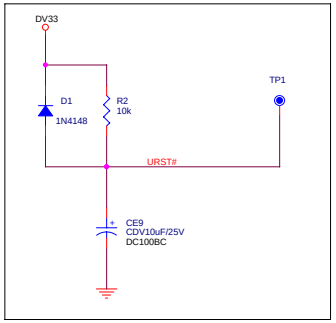








RESET Circuit



AZ1117	Rb	Ra
Fix regulator	0 ohm	OFF
Adj regulator	300 1%	680 1%

1.25x(1+Rb/Ra)

Note for Fix or Adj Regulator

Ra = 680 FOR 1.8V
Ra = 560 FOR 1.92V

2,3 DV33 DV33

MediaTek Confidential

MediaTek (ShenZhen) Inc.

Title	SLOTIN1389HD_TOHEI_HD62		
Size C	Document Number INDEX	Drawn: Tom Wang	Rev 1
Date: Saturday, October 29, 2005		Checked: Tom Wang	
		Sheet 1 of 5	

MT1389HD

Pin Assignment v1.5

SANYO
SF-HD62

2SK3018

2N3904

2SB1132

Very Important to reduce Noise

RS-232

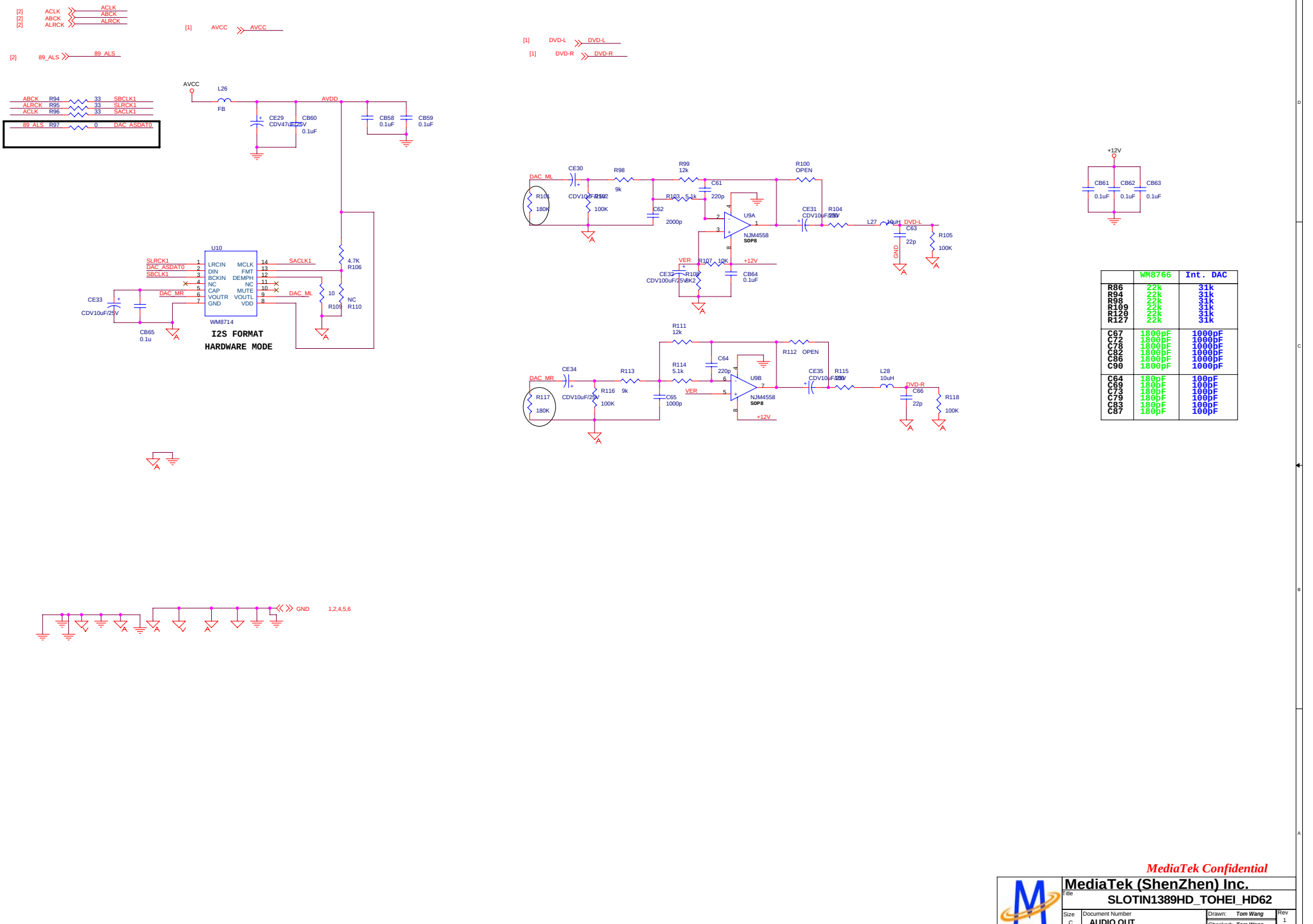
reserve this circuit for protection OPU

MediaTek Confidential

MediaTek (ShenZhen) Inc.

Title: SLOTIN1389HD_TOHEI_HD62

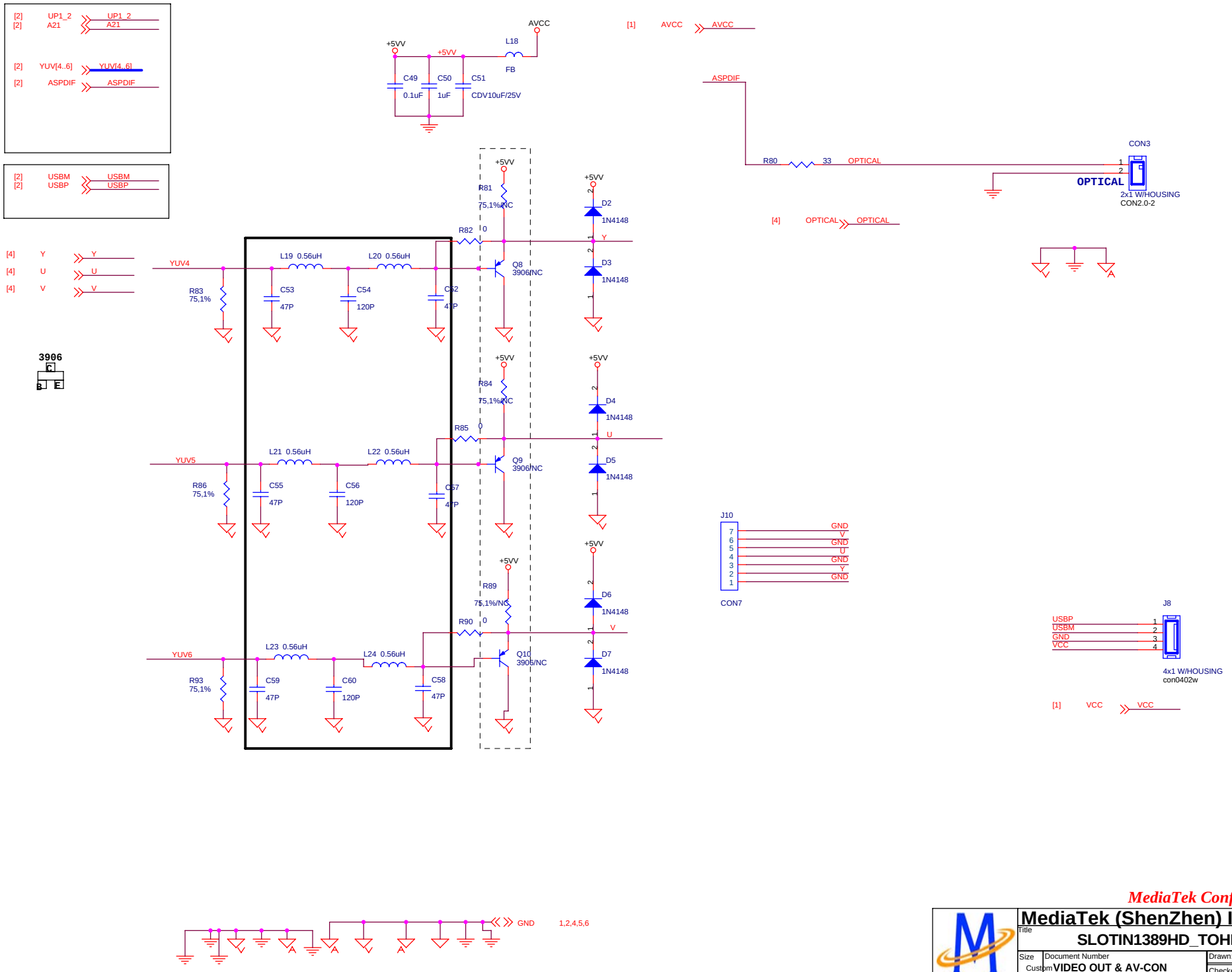
Size: Custom | Document Number: MT1389HD TQFP 256 | Drawn: Tom Wang | Checked: Tom Wang | Rev: 1 | Date: Saturday, October 29, 2005 | Sheet 2 of 5



	WM8766	Int. DAC
R86	22k	31k
R94	22k	31k
R98	22k	31k
R109	22k	31k
R120	22k	31k
R127	22k	31k
C67	1800pF	1000pF
C72	1800pF	1000pF
C78	1800pF	1000pF
C82	1800pF	1000pF
C86	1800pF	1000pF
C90	1800pF	1000pF
C64	180pF	100pF
C69	180pF	100pF
C73	180pF	100pF
C79	180pF	100pF
C83	180pF	100pF
C87	180pF	100pF

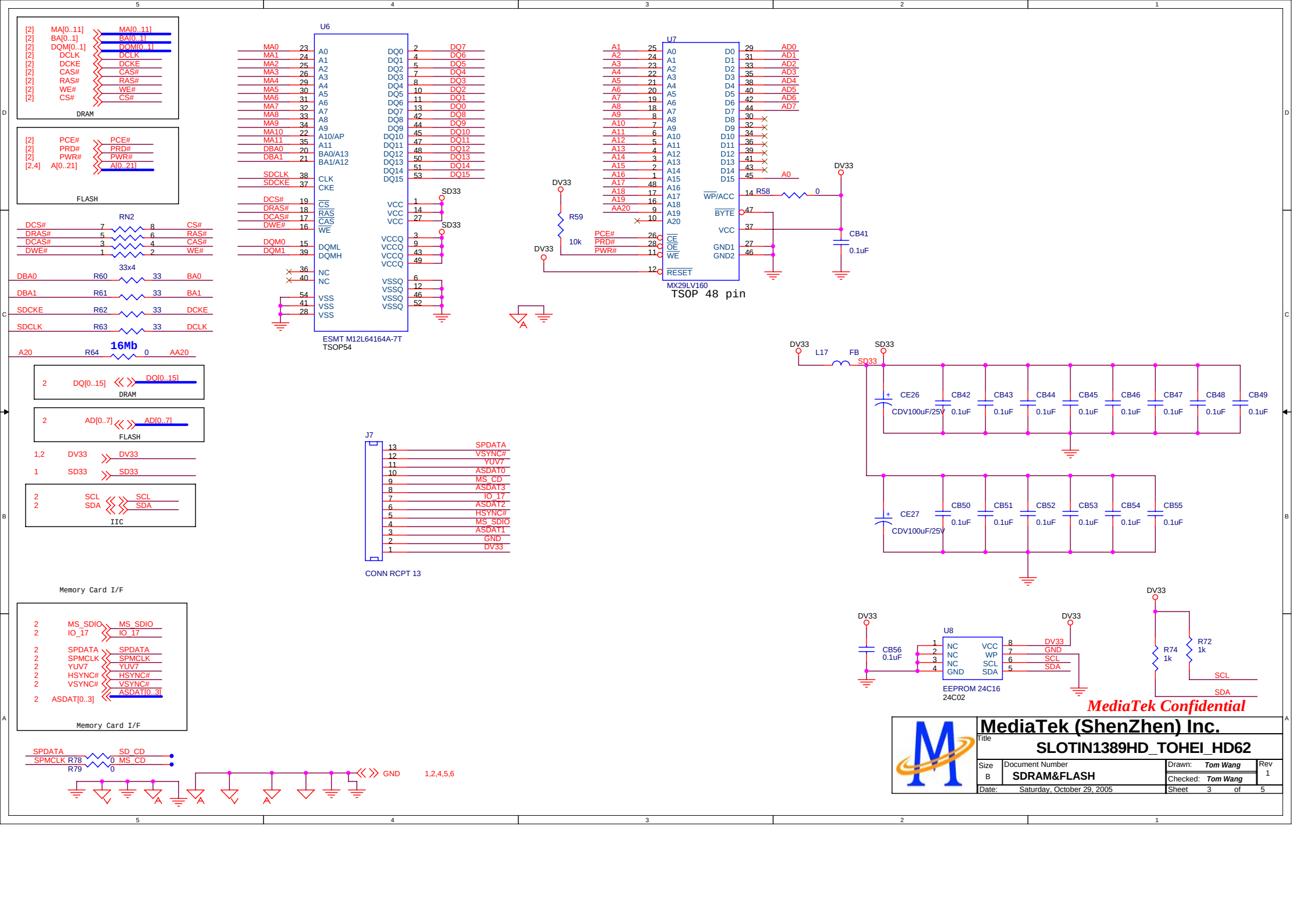
MediaTek (ShenZhen) Inc.

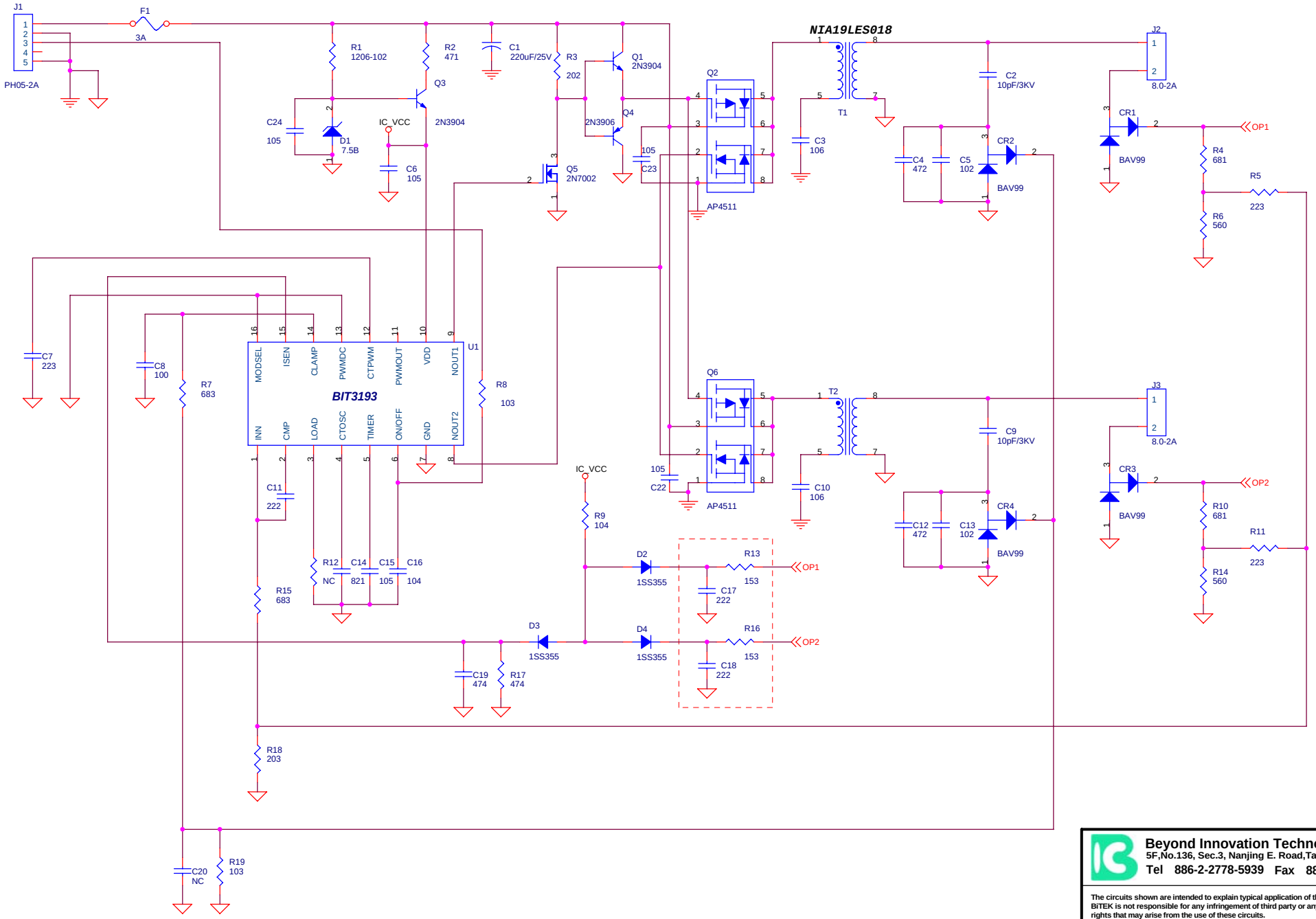
Title	SLOTIN1389HD_TOHEI_HD62		
Size: C	Document Number: AUDIO OUT	Drawn: Tom Wang	Rev: 1
		Checked: Tom Wang	
Date: Saturday, October 29, 2005		Sheet 5 of 5	



MediaTek Confidential

MediaTek (ShenZhen) Inc.			
Title: SLOTIN1389HD_TOHEI_HD62			
Size: Custom	Document Number: VIDEO OUT & AV-CON	Drawn: *Tom Wang*	Rev: 1
		Checked: *Tom Wang*	
Date: Saturday, October 29, 2005		Sheet 4 of 5	


DRAM
FLASH
RN2
33x4
16Mb
ESMT M12L64164A-7T
TSOP54
MX29LV160
TSOP 48 pin
CONN RCPT 13
IIC
Memory Card I/F
EEPROM 24C16
24C02
CDV100uF/25V
MediaTek Confidential
MediaTek (ShenZhen) Inc.
SLOTIN1389HD_TOHEI_HD62
SDRAM&FLASH
Tom Wang
Saturday, October 29, 2005



Beyond Innovation Technology Co., LTD.
5F,No.136, Sec.3, Nanjing E. Road,Taipei,Taiwan,R.O.C.
Tel 886-2-2778-5939 Fax 886-2-2778-1050

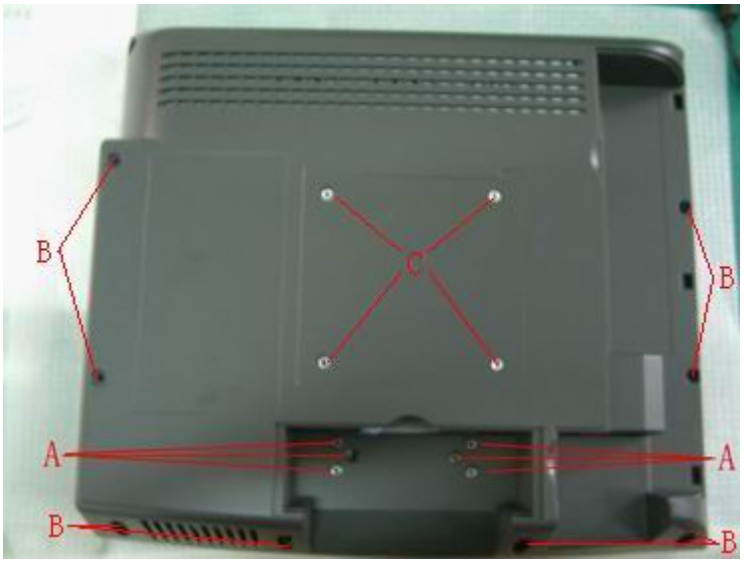
Title	BIT3193 2 LAMPS 2 TX H.B VER0.1FOR E-MAX		
Size: Custom	Document Number: INV537001020	Task Code: <Number>	Rev: 0.3
Date: Friday, March 17, 2006		Sheet 1 of 1	

Part 4 Disassemble/Assemble Procedure

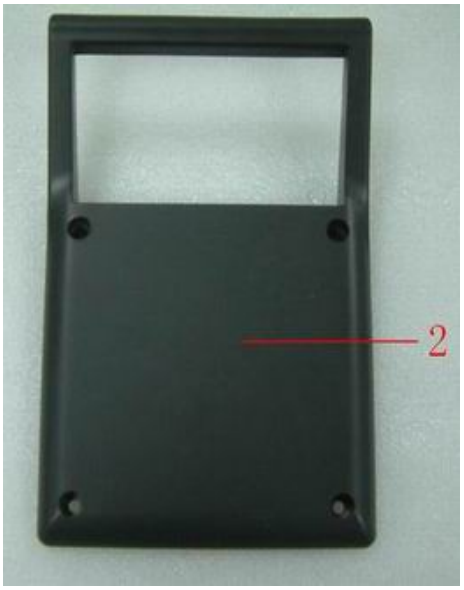
1. Fig1: Whole assembly diagram in which: LCD screen (1), bottom base (2), remote sensor (3), power indicator (4)

2. Fig2: Back view of the LCD TV without bottom base.

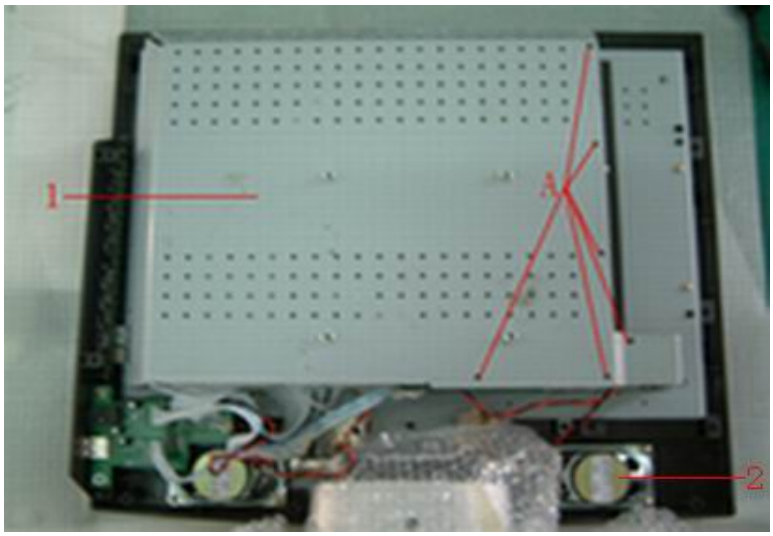
Remove six screws for bottom base fixing from (A) positions, screws for rear panel fixing from (B) positions and screws for handle fixing from (C) positions.



3. Fig3: Whole assembly diagram in which: Rear Panel (1), handle (2).

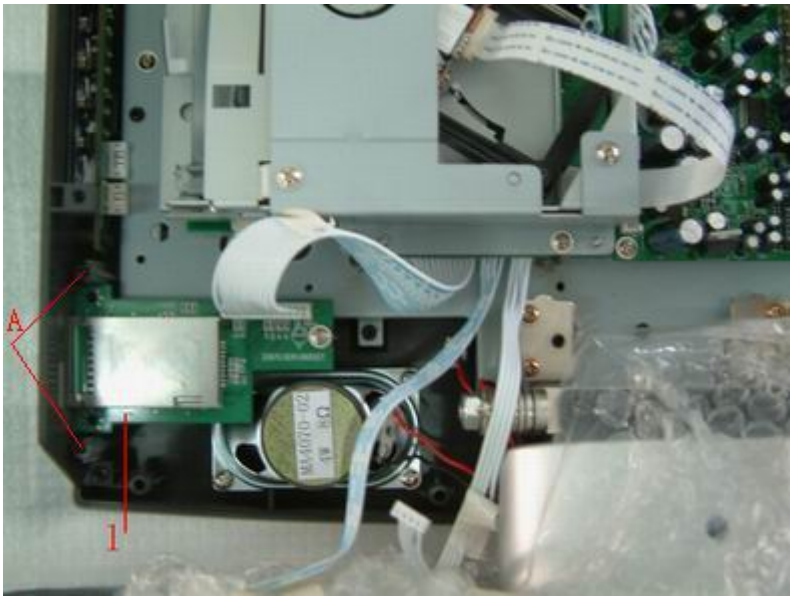


4. Fig4: Assembly diagram without the rear panel in which: shield A (1), speaker (2).
   Remove the screws from (A) positions.



5. Fig5: Assembly diagram without shield A in which: Main board (1), Power board (2), DVD board (3), Keypad board (4), USB and Headphone board (5), shield B (6).

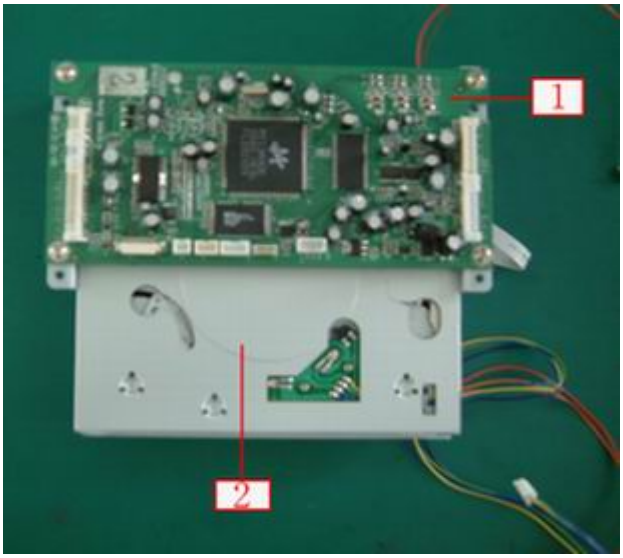
6. Fig6: remove the USB and Headphone board to see the Card board (1). Remove the screws for USB and Headphone board fixing from the (A) positions.

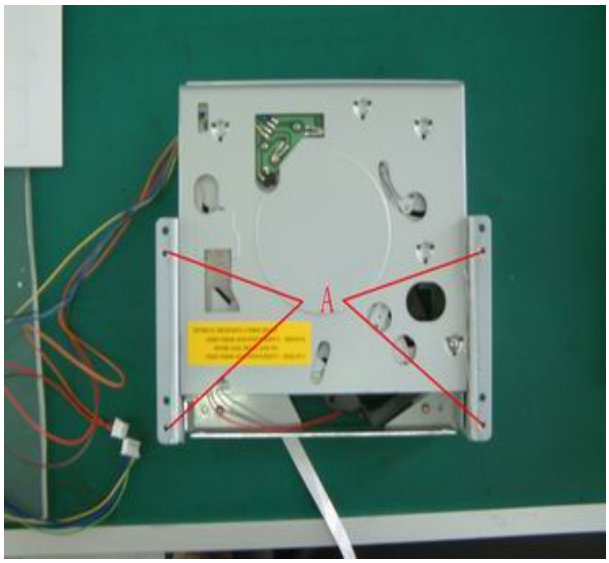


7. Fig7: Remove DVD board to see the HI-voltage Board (1). Remove the screws for DVD board fixing from (B) positions.

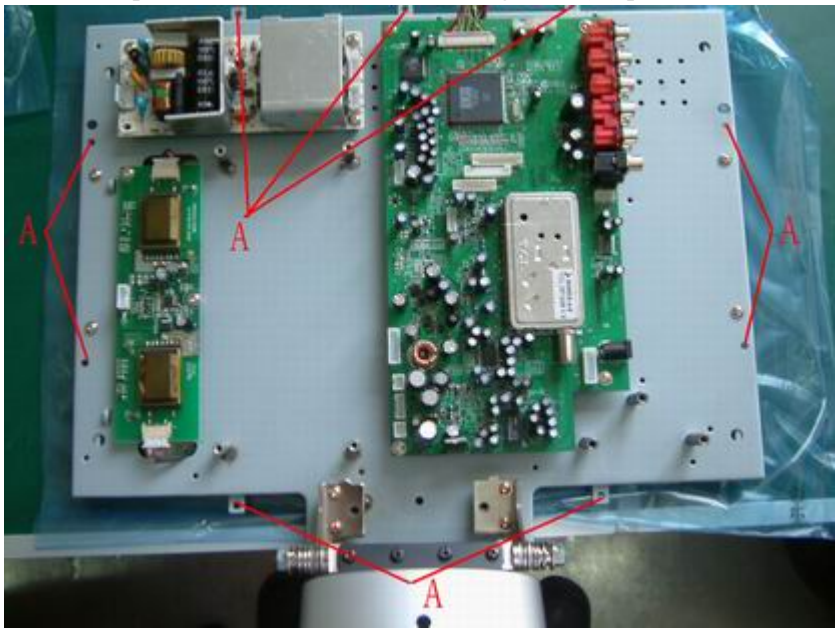
Remove the Card board and the screws for its fixing from (A) positions.

8. Fig8: Whole Assembly diagram in which: DVD board (1), DVD Loader (2).
Remove the screws for DVD board and loader fixing from (A) positions.

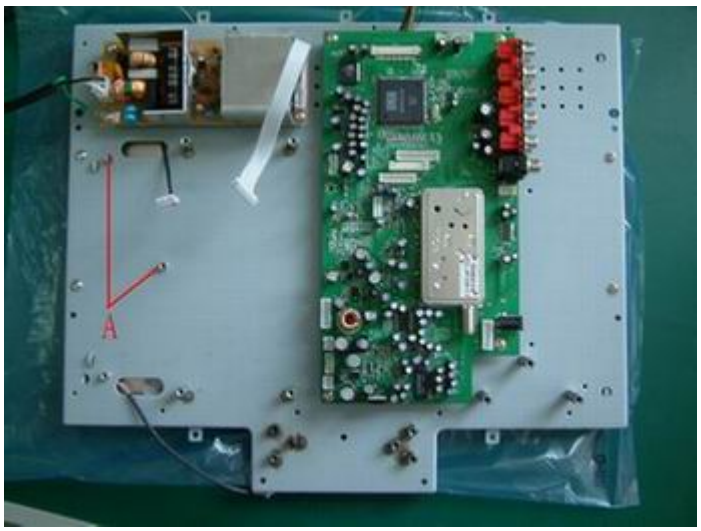




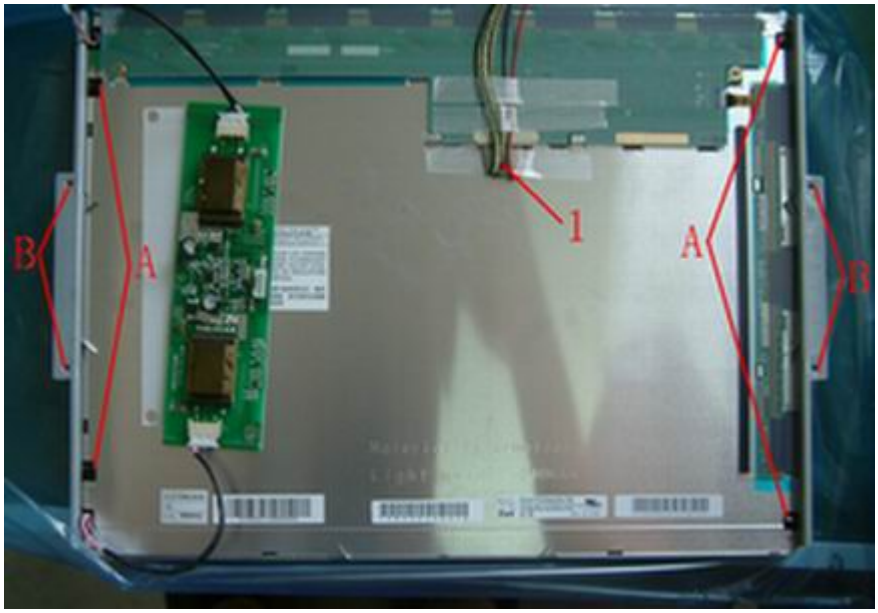
9. Fig9: Remove the front panel and the screws for its fixing from (A) positions.



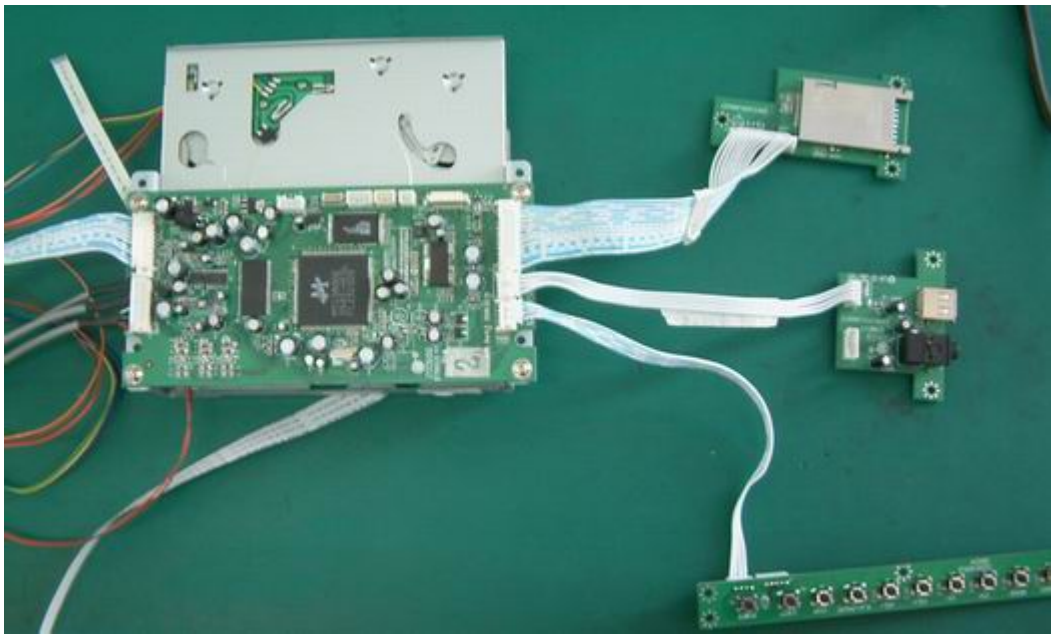
10. Fig10: Remove the HI-voltage Board and the screws for its fixing from(A) positions and remove the base.



11. Fig11: The LCD Screen, HI-voltage Board and LVDS (1).
    Remove the screws for screen fixing to shield from (A) positions.
    Remove the screws for screen fixing to front panel from (B) positions.



12. Fig13: The connections between DVD board and Card board, USB and Headphone board, Key pad board.



Part 5 Part list of TEACLCDV1501M

No.	Serial number of material	Specification	QNTY	Position
		Plastic molding pieces		
1	01.00.SJ.LTD61501.E001	LTD61501-front panel	1	LTD-61501-RE001
2	01.00.SJ.LTD61501.E002	LTD61501-middle panel (black)	1	LTD-61501-RE002
3	01.00.SJ.LTD61501.E003	LTD61501-rear panel	1	LTD-61501-RE003
4	01.00.SJ.LTD61501.E004	LTD61501-side panel	1	LTD-61501-RE004
5	01.00.SJ.LTD61501.E005	LTD61501-bottom base	1	LTD-61501-RE005
6	01.00.SJ.LTD61501.E006	LTD61501-cover of rotating axes	1	LTD-61501-RE006
7	01.00.SJ.LTD61501.E007	LTD61501-cover for lines output	1	LTD-61501-RE007
8	01.00.SJ.61901.E004	LTD61901-handle	1	LTD61901ZPTG-RE04
9	01.00.SJ.61901.E006	LTD61901-function keystoke	1	LTD61901ZPTG-RE06
10	01.00.SJ.61901.E007	LTD61901-indicator transparency	1	LTD61901ZPTG-RE07
11	01.00.SJ.61901.E008	LTD61901-remote control signal receiver transparency	1	LTD61901ZPTG-RE08
		Metals parts		
12	01.00.WJ.TJ.E753	LTD61501-LCD shield	1	LTD-61501-PT01
13	01.00.WJ.TJ.E754	LTD61501-DVD loader fixing frame	1	LTD-61501-PT02
14	01.00.WJ.TJ.E755	LTD61501-right shield panel	1	LTD-61501-PT03
15	01.00.WJ.TJ.E756	LTD61501-lower shield panel	1	LTD-61501-PT04
16	01.00.WJ.TJ.E757	LTD61501-shield cover	1	LTD-61501-PT05
17	01.00.WJ.TJ.E758	LTD61501-bottom panel	1	LTD-61501-PT06
18	01.00.WJ.TJ.E759	LTD1510-LCD fixing frame	2	LTD1510-PT16
19	01.00.WJ.TJ.E760	LTD61901-bracket of bottom base	1	LTD61901PT-011
20	01.00.WJ.TJ.E318	6600-grounding patch	1	G1(used for Power board)
		Radiator		
21	01.00.WJ.TJ.E268	28*28*10mm	1	
22	01.00.WJ.TJ.E761	41*54*30*25MM	1	used for Power board
23	01.00.WJ.TJ.E762	25*54*25*41MM	1	used for Power board

阻尼转轴				
24	01.32.ZZ.E125	LTD-61501	1	
Magnetism ring				
25	01.13.L.H.E002	22*14*6.5	1	Tuner commutator
Screw				
26	01.00.WJ.JG.E321	3*8PAHO	32	front panel and middle panel (8), LCD shield and front panel (10), Card board and middle panel (3), Keystoke board and side panel (5), USB board and middle panel (2),Remote control board and front panel(2), LCD shield and middle panel (2).
27	01.00.WJ.JG.E717	3*4PWBTTNI	29	LCD fixing frame and LCD shield (4), loader frame and DVD board (4), lower panel of shield and LCD shield (4), right panel and LCD shield (3), shield cover(14)
28	01.00.WJ.JG.E517	4*12 PMHO	4	rotating axes and bracket of bottom base
29	01.00.WJ.JG.E390	3*6PAHO	12	speaker and middle panel(8),right panel of shield and jack of Main board (4)
30	01.00.WJ.JG.E311	3*5PWMNI W=7.4	27	Main board and LCD shield (5),Power board and LCD shield (4), TFT driver board and LCD shield (3), LCD Screen and LCD fixing frame (4), loader and loader frame (4), loader frame and LCD shield (4), VGA board and LCD shield (3)
31	01.00.WJ.JG.E388	4*12PAHO	12	front panel and rear panel
32	01.00.WJ.JG.E519	4*6 KMHO	4	bracket of bottom base and bottom panel
33	01.00.WJ.JG.E520	3*6 KBHO	6	bottom panel and bottom base
34	01.00.WJ.JG.E675	3*10PAHO	2	side panel and front panel
35	01.00.WJ.JG.E718	4*8 PMHO	6	rotating axes and LCD shield
36	01.00.WJ.JG.E719	4*10 PMHO	4	handle and shield cover
37	01.00.WJ.JG.E721	3*5 CBANI	3	matchingU1,D3,D4(used for Power board)
底壳表牌				
38	01.00.BP.DZ.E000	According to customer's choice	1	
机芯仓门条				
39	01.00.DP.JY.E135	LTD-1510	1	
Module of DVD loader				
40	01.15.JX.ETDS208SVB	TD-S208S-SV-B(long line)	1	
LCD Screen				

41	01.17.LCD.E15SGD	15 " Shanghai SVA-NEC liquid crystal display screen	1	
		Speaker		
42	01.00.SP.E089	LD7040A-027-1(8Ω 3W)	2	
		Remote Controller		
43	01.00.RC.RC6043	RC-6043	1	
		车载适配器(成品)		
44	02.02.MCA-60	MCA-60	1	According to customer's choice
		Alkalescence battery		
45	01.14.DX.B.E0007	7#	1	
		Commutator		
46	01.40.CON.DDZ.E001	N 制 775-41207-00	1	
		扎线带		
47	01.47.CNT.LJX.5.E015		1	电源线扎线带
		扎线扣		
48	01.00.FZ.QT.E122	12CM	2	
		AC Power line		
49	01.47.CNT.ACX.E077	355+LASR-85	1	Power board to external power supply
		射频线		
50	01.47.CNT.CTX.E106	RCA＋公制 F 头(L190mm)	1	
		LVDS connections bus		
51	01.47.CNT.LJX.2.E138	1.25-20P-1.25-20P-150mm	1	
		Connections bus		
52	01.47.CNT.LJX.7.E325	2.0-4Y-4Y-140MM Contrary	1	VGA board to Main board
53	01.47.CNT.LJX.7.E326	2.0-11Y-11Y-230MM Contrary (shield)	1	VGA board to Main board
54	01.47.CNT.LJX.7.E327	2.0-5Y-5Y-460MM Contrary (shield)	1	Keystoke board to Main board
55	01.47.CNT.LJX.7.E328	2.0-4Y-4Y-190MM Same	1	Keystoke board to DVD board

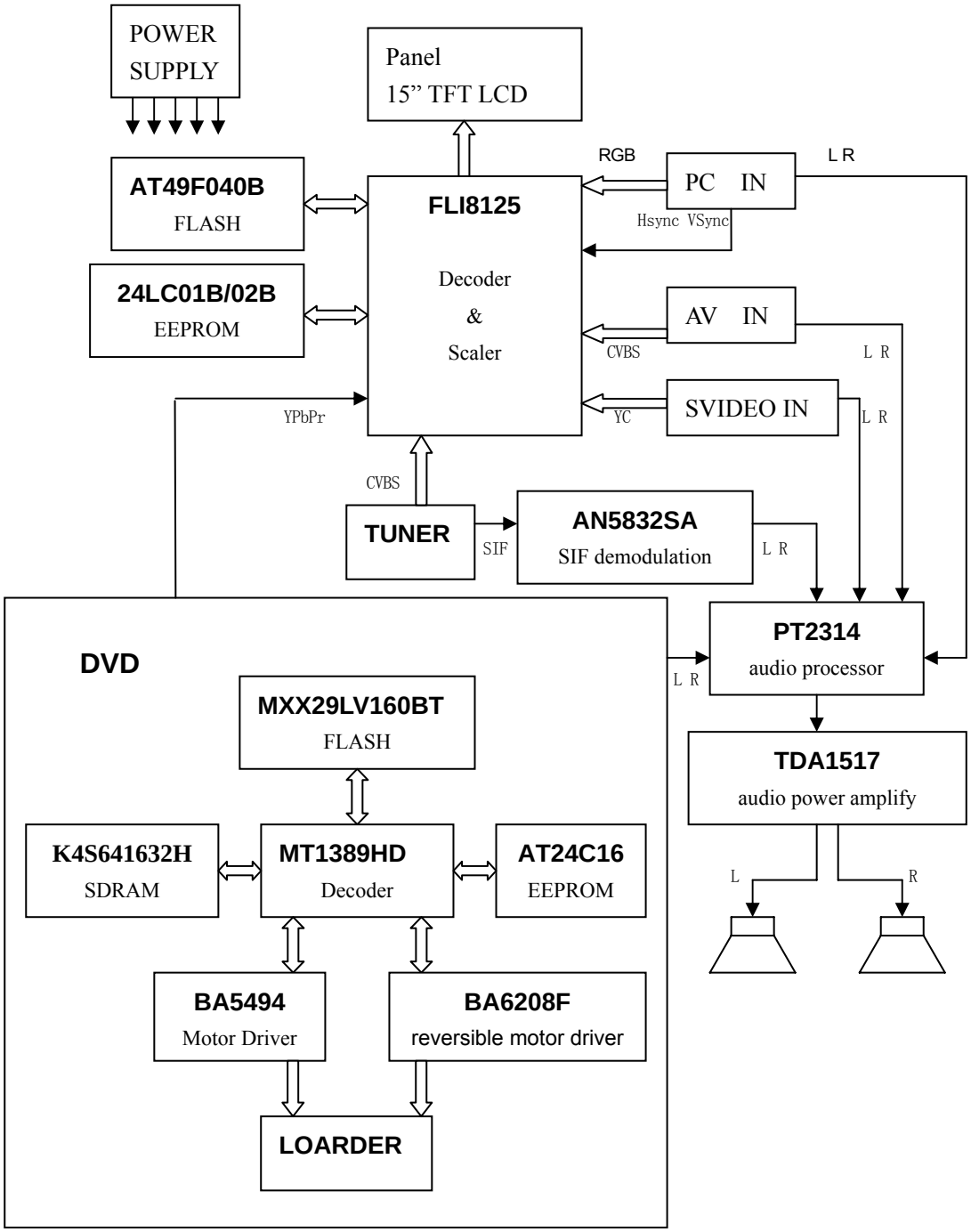
56	01.47.CNT.LJX.7.E329	2.0-5Y-5Y-210mm Contrary	1	Headphone board to Main board
57	01.47.CNT.LJX.7.E330	2.0-4Y-4Y-150MM Contrary	1	Headphone board to DVD board
58	01.47.CNT.LJX.7.E331	2.0-13Y-13Y-140MM Contrary	1	Card board to DVD board
59	01.47.CNT.LJX.7.E188	2.0-5Y-5Y-260MM Same	1	TFT driver board to Main board
60	01.47.CNT.LJX.7.E332	2.0-10Y-10Y-140MM Contrary	1	DVD board to Main board
61	01.47.CNT.LJX.7.E333	2.0-11Y-11Y-140mm Contrary (shield)	1	DVD board to Main board
62	01.47.CNT.LJX.7.E334	2.54-6Y-6Y-180MM Same	1	Power board to Main board
63	01.47.CNT.LJX.7.E335	2.54-6Y-6Y-140MM Same	1	Inner of Main board
Flat bus				
64	01.48.BPX.2.E025	0.5*24P*220mmB	1	Loader to DVD board

No.	Serial number of material	Name and type	Specification	QNTY	Position
Assemblies					
65	01.00.DP.XJ.E172	Silica gel pad	LTD-2030 脚 垫（10*15*7.8MM）black	6	
66	01.00.DP.JY.E124	绝缘粒子	TO-220	1	matching U1(used for Power board)
67	01.00.DP.QT.E001	垫片	sil-pad 400-2820	1	matching U1(used for Power board)
68	01.00.DP.JY.E183	Insulation pad	145*44*0.5mm(single side glue) black	1	Insulation pad for TFT driver board
Circuit boards					
69	02.11.LTD06M3227C01	Main board	LTD06M-3227C01	1	
70	02.15.LTD06K3228C01	Keystoke board	LTD06K-3228C01	1	
71	02.22.LTD06T3229C01	TV board	LTD06T-3229C01	1	
72	02.14.LTD06I3230C01	VGA board	LTD06I-3230C01	1	
73	02.14.LTD06I3307C01	Card board	LTD06I-3307C01	1	
74	02.14.LTD06I3308C01	USB and Headphone board	LTD06I-3308C01	1	
75	02.23.LTD06V2805C01	DVD board	LTD06V-2805C01	1	
76	02.19.LTD06P2956C01	Power board	LTD06P-2956C01	1	
77	02.07.MINV1507SVA1B01	HI-voltage Board	MINV15-07SVA1B01	1	
Accessories					
78	01.00.BP.DC.E000	电池表牌	According to customer's	1	

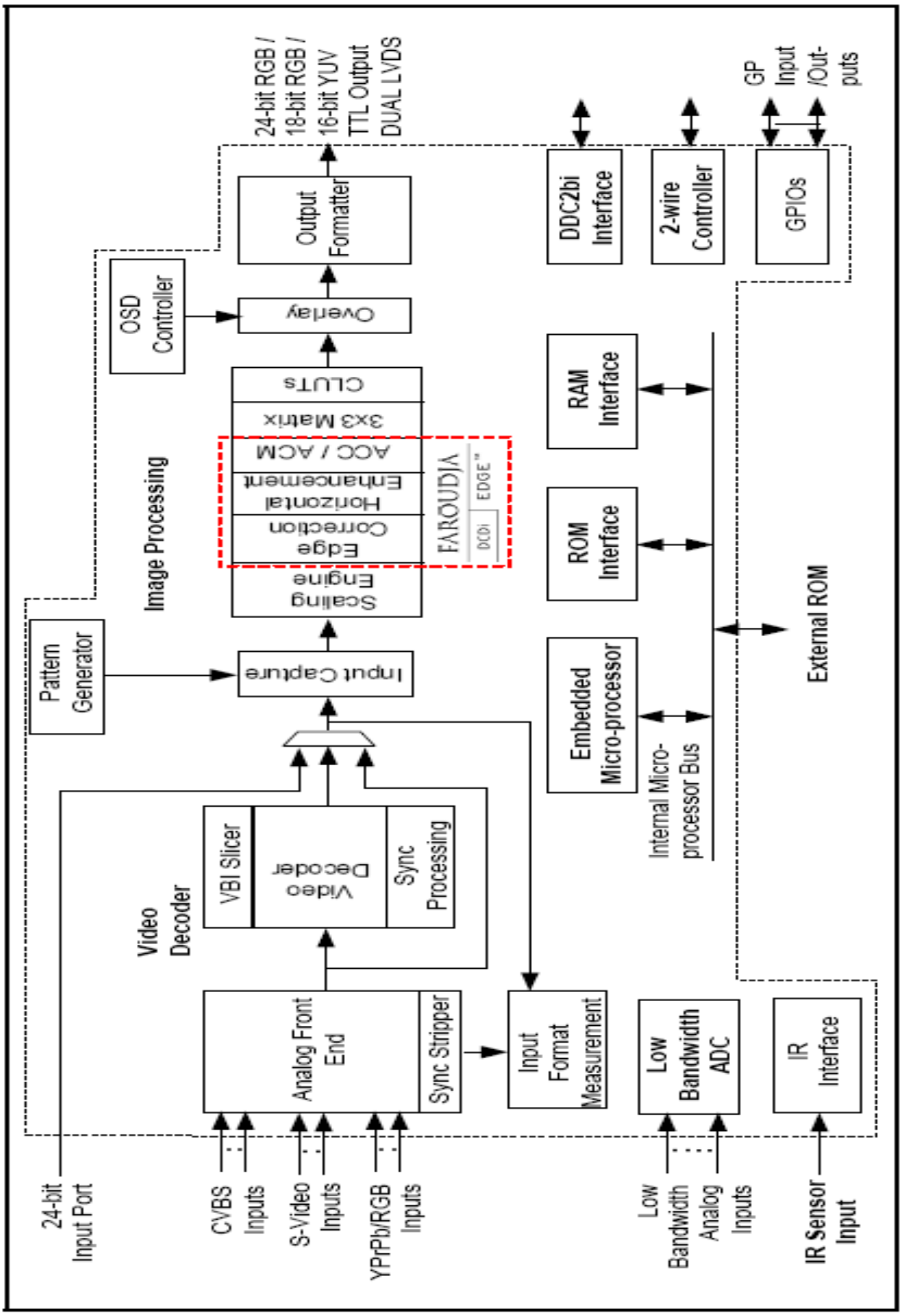
			choice		
79	01.00.YS.SM1.E000	User's manual	According to customer's choice	1	
80	01.00.YS.ZX2.E000	Packing list	According to customer's choice	1	
81	01.00.YS.TZ.M.E000	Bar code	According to customer's choice	1	
82	01.00.YS.FY3.E049	Certificate		1	
83	01.00.YS.SC.E002	Warranty card	Warranty card	1	
84	01.00.BZ.X.W.E000	Package box	According to customer's choice	1	
85	01.00.BZ.X.B.E000	White box	According to customer's choice	1	
86	01.00.DP.QT.E016	EPE cushion	LTD-61501	1	
87	01.00.BZ.D.H.E004	环保袋	15*33cm	1	Packing bag for VGA line
88	01.00.BZ.D.H.E029	环保袋	6*23cm	2	Packing bag for VGA line, Packing bag for S-Video line
89	01.00.BZ.D.H.E002	环保袋	11*28cm	2	Packing bag for power adapter line, Packing bag for power line
90	01.00.BZ.D.H.E163	环保袋	9*33CM	1	Packing bag for remote controller
91	01.00.BZ.D.H.E198	无纺布	58*75CM	1	Packing bag for the machine
92	01.00.BZ.D.Z.E035	自封袋	7.5*8CM	1	Packing bag for 7# battery

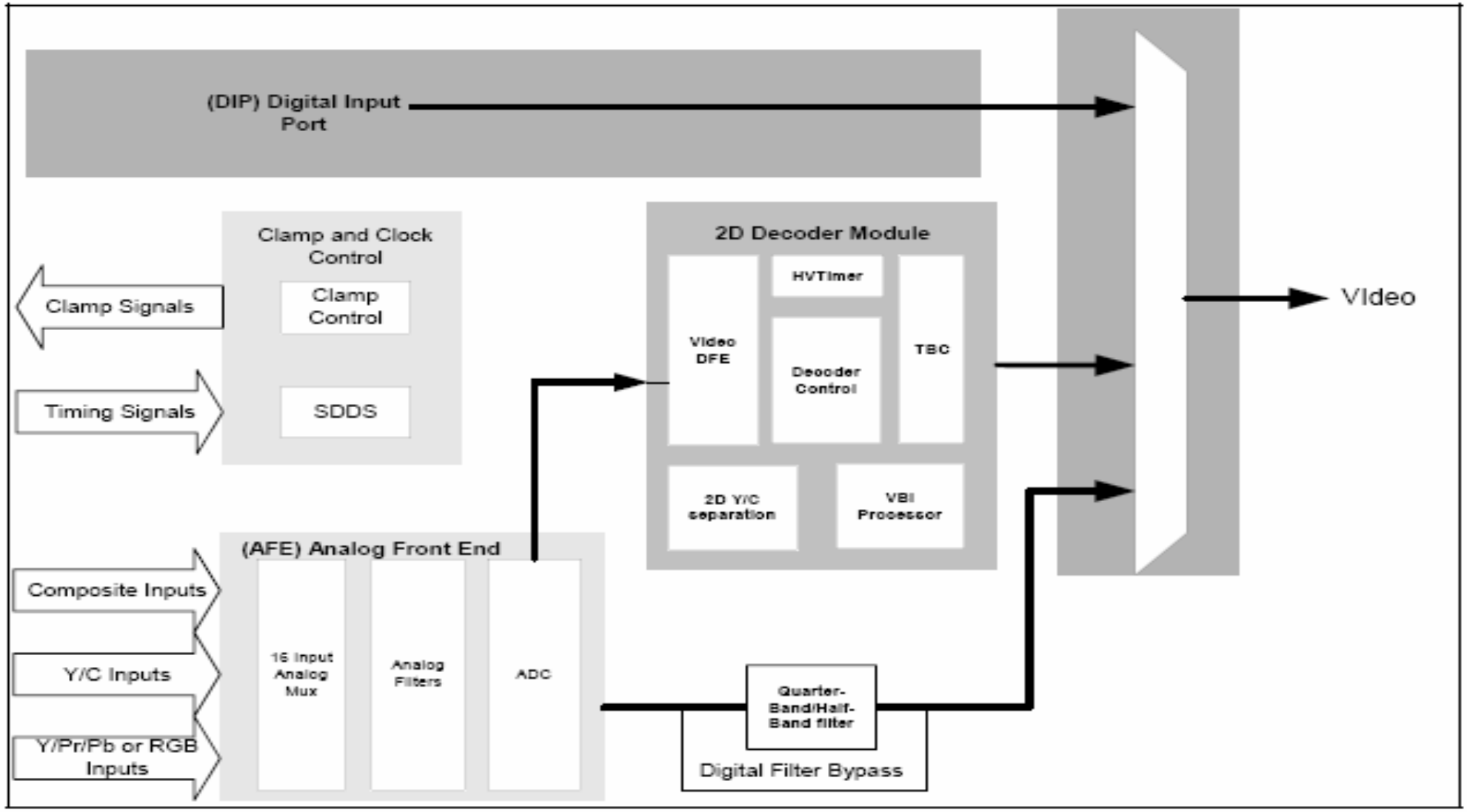
Part 6 Debugging Procedures

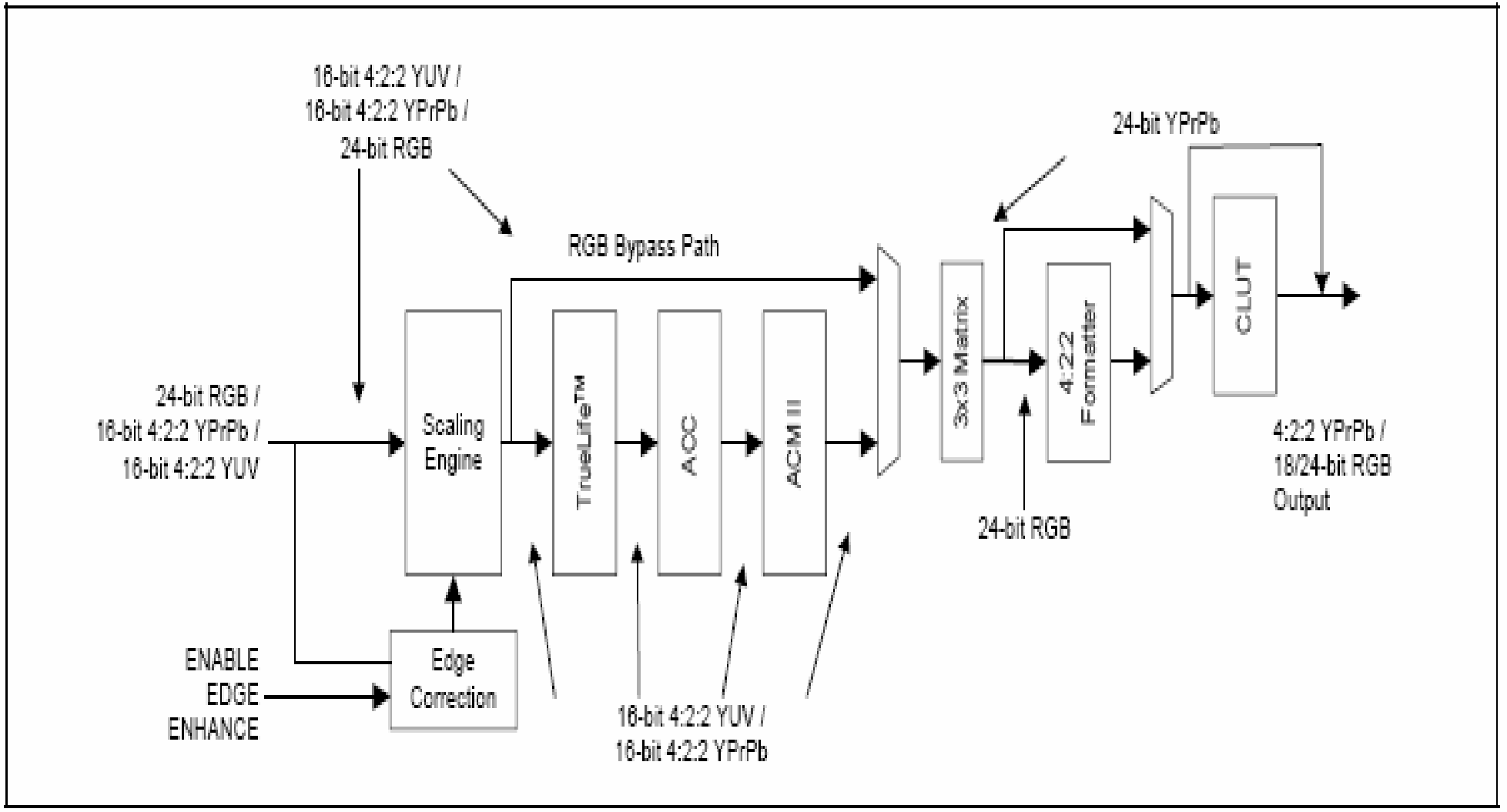
1. Workflow Of The System



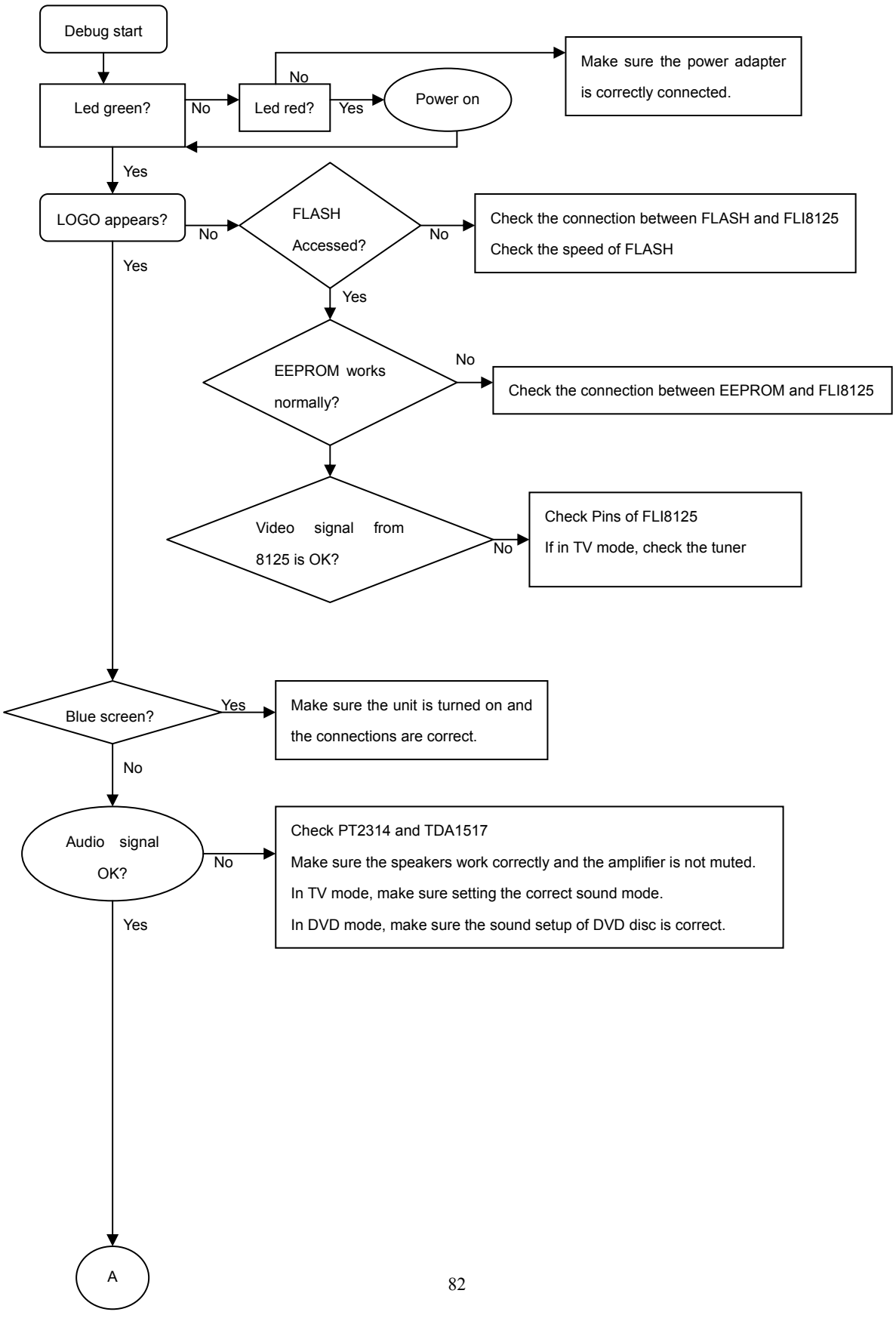
2. Signal process diagram

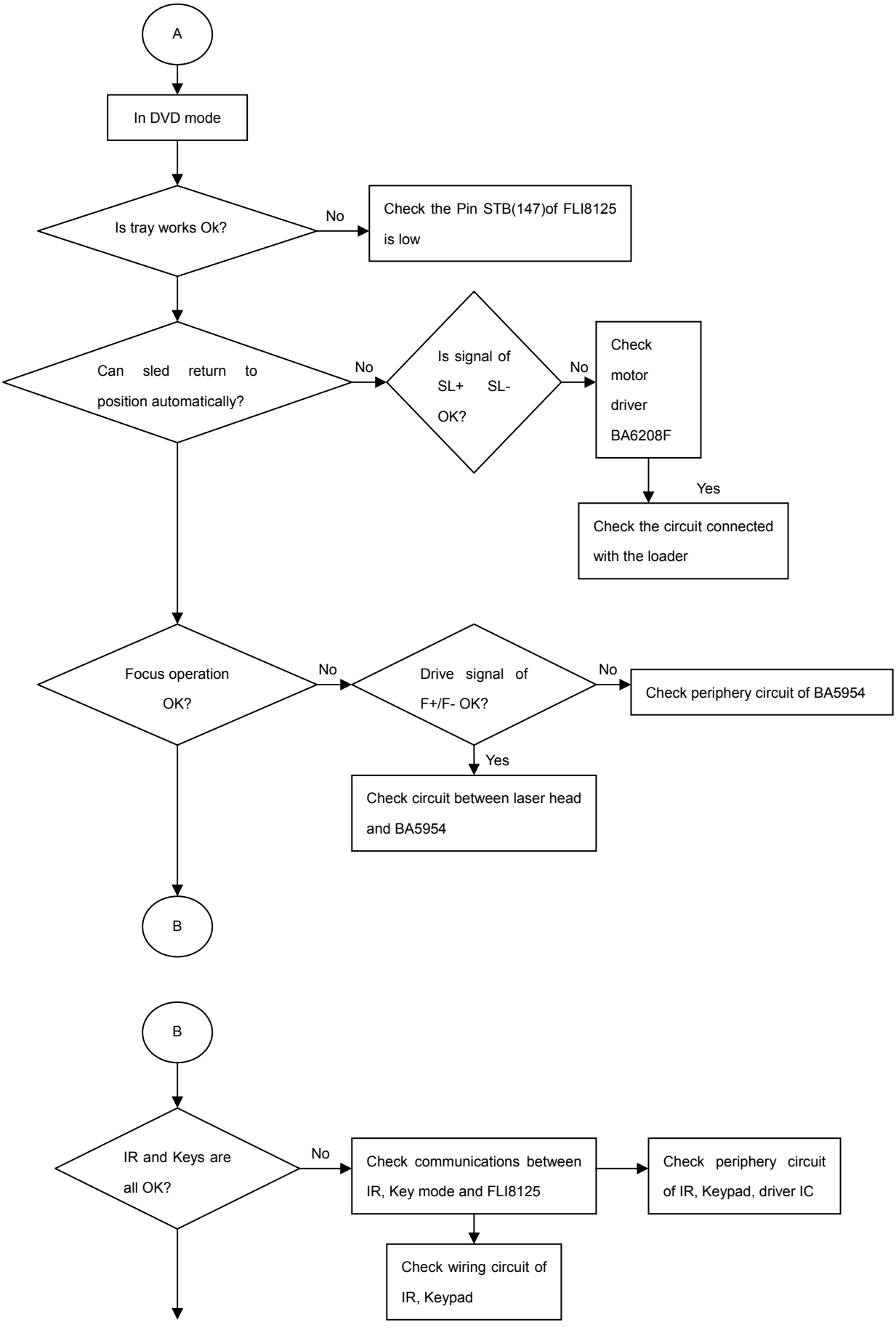


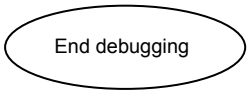

(DIP) Digital Input Port
Clamp and Clock Control
Clamp Signals
Clamp Control
Timing Signals
SDDS
2D Decoder Module
HVTimer
Video DFE
Decoder Control
TSC
2D Y/C separation
VBI Processor
Video
(AFE) Analog Front End
Composite Inputs
Y/C Inputs
Y/Pr/Pb or RGB Inputs
16 Input Analog Mux
Analog Filters
ADC
Quarter-Band/Half-Band filter
Digital Filter Bypass


16-bit 4:2:2 YUV /
16-bit 4:2:2 YPrPb /
24-bit RGB
24-bit YPrPb
RGB Bypass Path
24-bit RGB /
16-bit 4:2:2 YPrPb /
16-bit 4:2:2 YUV
Scaling Engine
TrueLife™
ACC
ACM II
3x3 Matrix
4:2:2 Formatter
CLUT
4:2:2 YPrPb /
18/24-bit RGB
Output
24-bit RGB
ENABLE
EDGE
ENHANCE
Edge Correction
16-bit 4:2:2 YUV /
16-bit 4:2:2 YPrPb

3. Debugging Strategy




A
In DVD mode
Is tray works Ok?
No
Check the Pin STB(147)of FLI8125 is low
Can sled return to position automatically?
No
Is signal of SL+ SL- OK?
No
Check motor driver BA6208F
Yes
Check the circuit connected with the loader
Focus operation OK?
No
Drive signal of F+/F- OK?
No
Check periphery circuit of BA5954
Yes
Check circuit between laser head and BA5954
B
B
IR and Keys are all OK?
No
Check communications between IR, Key mode and FLI8125
Check periphery circuit of IR, Keypad, driver IC
Check wiring circuit of IR, Keypad



4. Tips Of Some Typical Troubleshooting

White screen

First check voltage in HI-voltage Board; otherwise check the voltage of MAIN board , if abnormal , the problem occurs in 1U2. If the voltage is OK, check the LVDS. At last the connection between the main board and drive board may be the target for troubleshooting.

Black screen

This problem often arise from the voltage input to the screen, so the first step is to check the voltage of invert circuit. Otherwise check if the status is standby. If in TV mode, check the power for tuner is correct.

No color

Check if the connection with the external device is correct. Otherwise make sure the saturation is not zero. At last the problem may arise from the FLI8125.

Abnormal picture

Check if the range of the signal input to FLI8125 is correct. If no, the problem may be in the AFE(Analog Front End). Otherwise make sure the color system is correct. Then check the LVDS and the LCD Screen.

Pictures with no sound

Firstly, make sure the speakers works well. If so, the trouble mostly occurred in TDA1517 in 3U5 in main board, then PT2314 in 3U4.

Sounds with no picture

Check if any signal inputs to FLI8125, if yes, the problem may be in the AFE. Otherwise check the LVDS.