PIONEER®
The Art of Entertainment

Service Manual

SERVICE GUIDE

ORDER NO.
RRV1896

DVD PLAYER
DV-505
DV-S9

DVD LD PLAYER
DVL-909

CONTENTS

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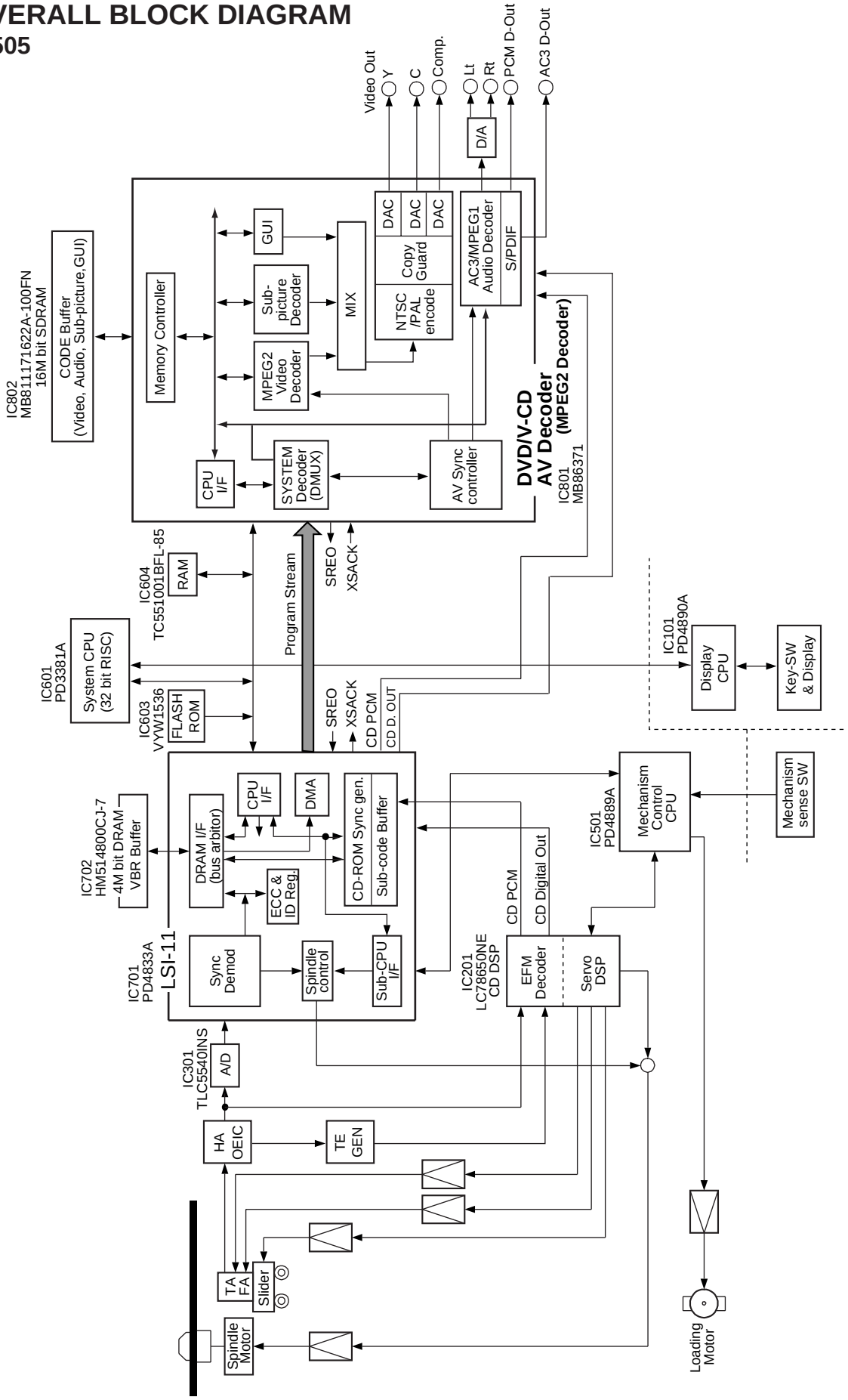
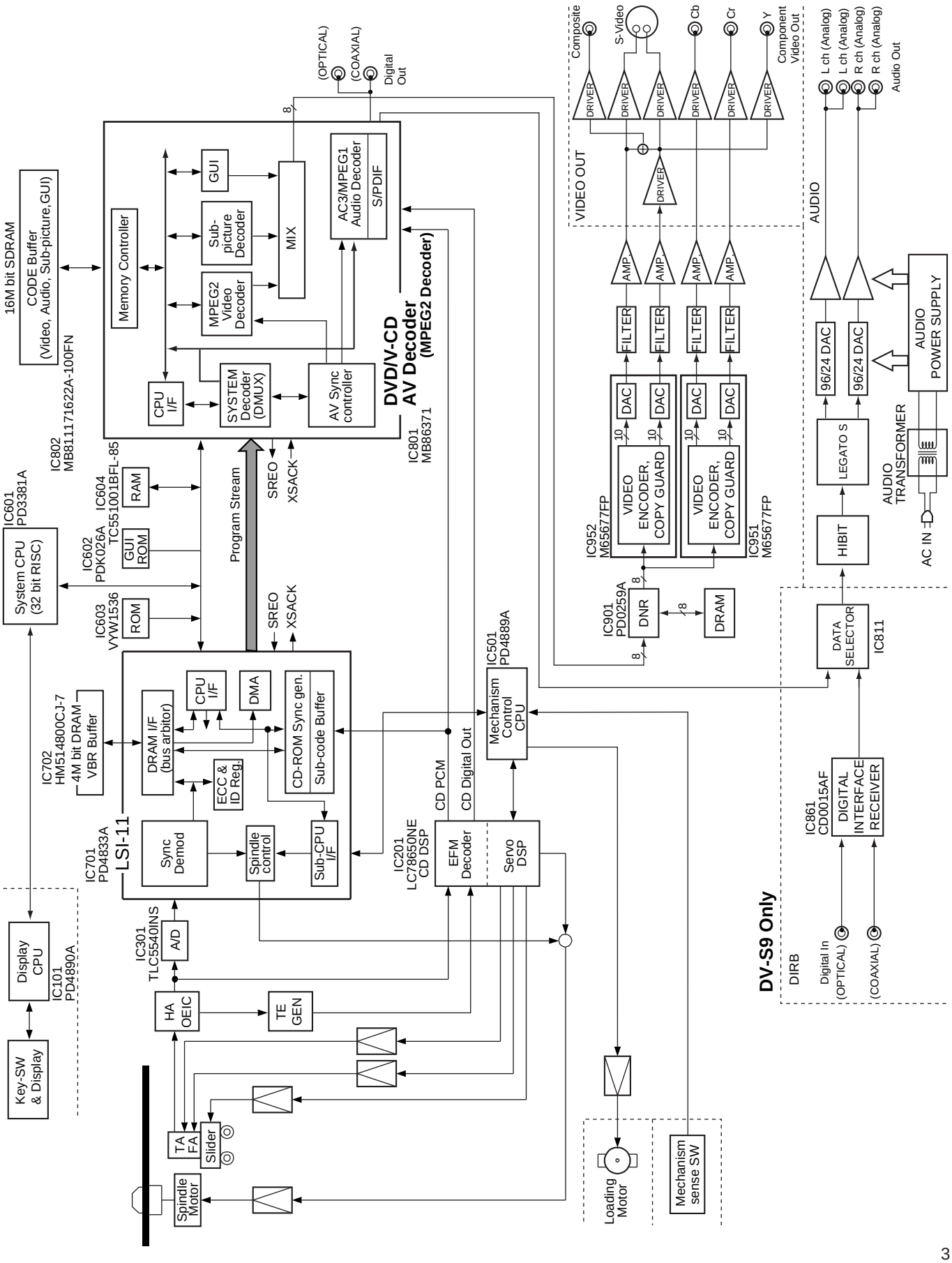
1. CIRCUIT DESCRIPTION

1.1 OVERALL BLOCK DIAGRAM

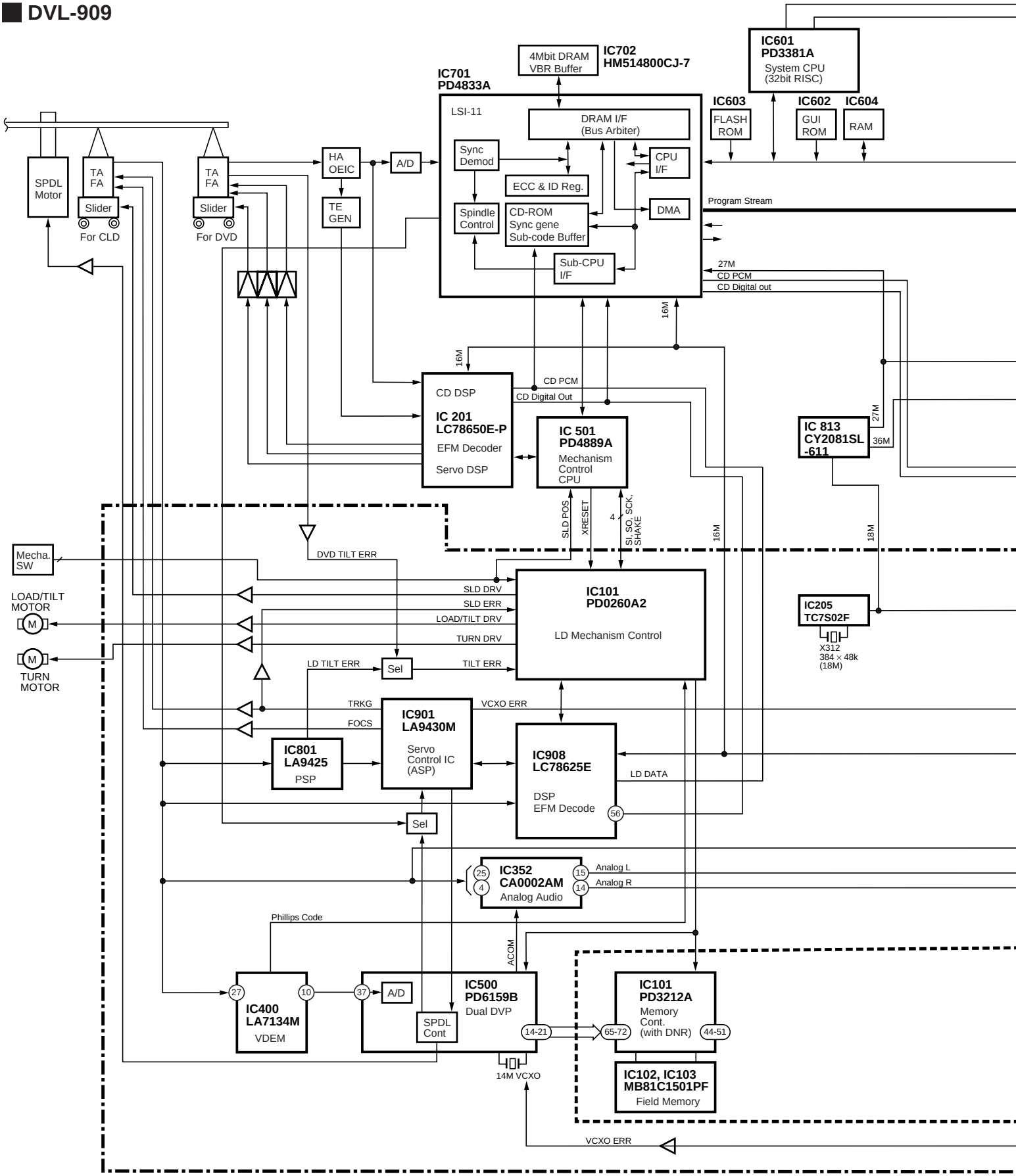
DV-505

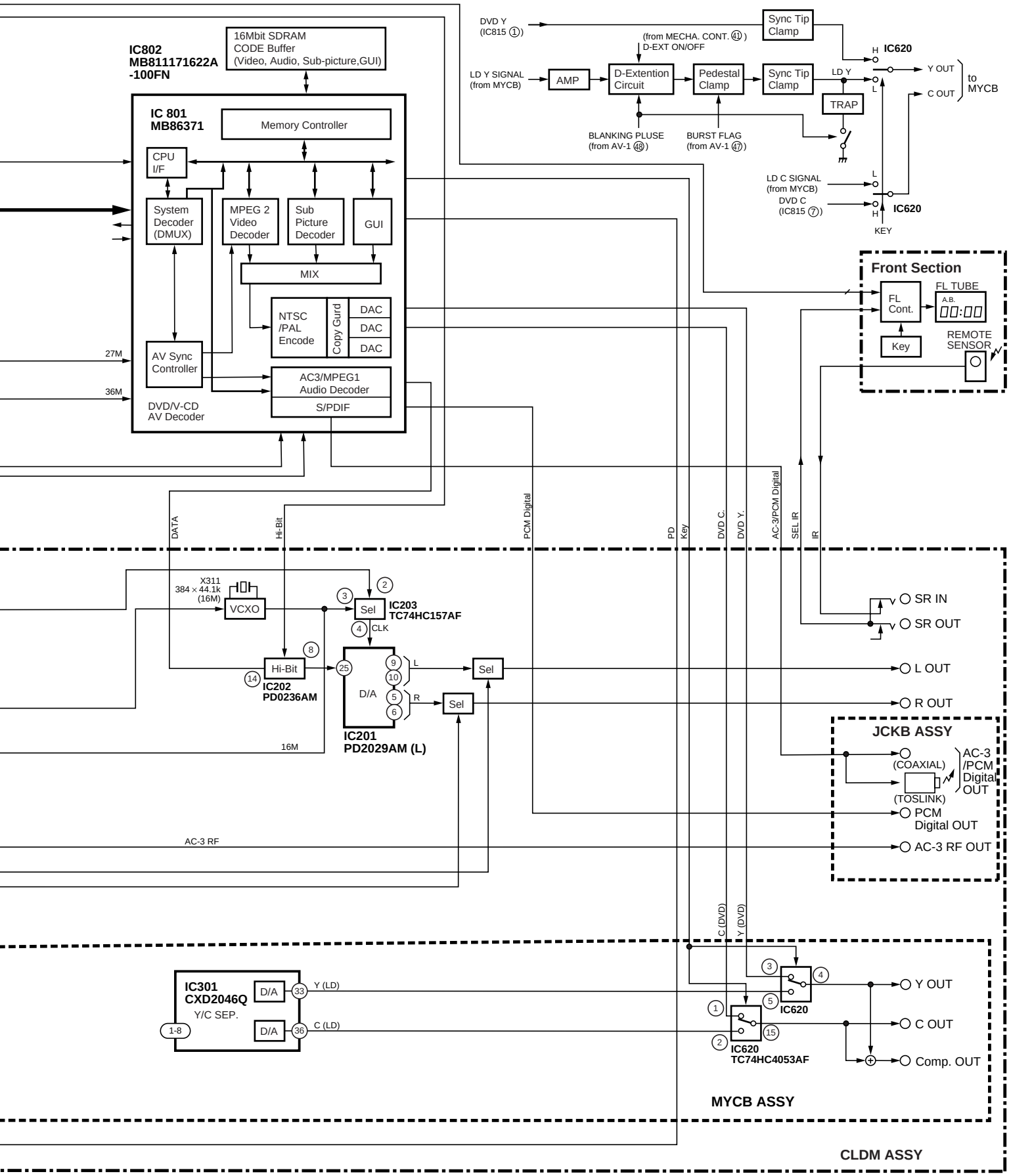


DV-S9 and DV-09



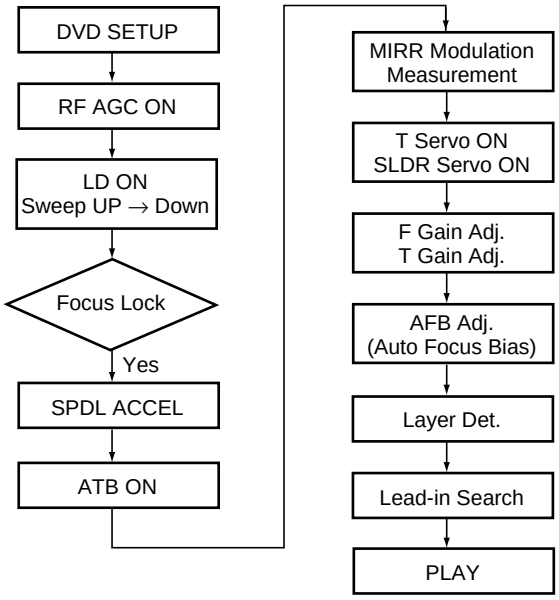
DVL-909


IC601
PD3381A
System CPU
(32bit RISC)
4Mbit DRAM
VBR Buffer
IC702
HM514800CJ-7
IC701
PD4833A
LSI-11
IC603
FLASH ROM
IC602
GUI ROM
IC604
RAM
DRAM I/F
(Bus Arbiter)
Sync Demod
CPU I/F
ECC & ID Reg.
Spindle Control
CD-ROM Sync gene Sub-code Buffer
DMA
Sub-CPU I/F
Program Stream
27M
CD PCM
CD Digital out
16M
SPDL Motor
TA FA
Slider
For CLD
For DVD
HA OEIC
A/D
TE GEN
CD DSP
IC 201
LC78650E-P
EFM Decoder
Servo DSP
IC 501
PD4889A
Mechanism Control CPU
IC 813
CY2081SL-611
36M
SLD POS
XRESET
SI, SO, SCK, SHAKE
4
18M
Mecha. SW
DVD TILT ERR
LOAD/TILT MOTOR
TURN MOTOR
SLD DRV
SLD ERR
LOAD/TILT DRV
TURN DRV
IC101
PD0260A2
LD Mechanism Control
IC205
TC7S02F
X312
384 × 48k
(18M)
LD TILT ERR
Sel
TILT ERR
TRKG
FOCS
VCXO ERR
IC901
LA9430M
Servo Control IC (ASP)
IC801
LA9425
PSP
IC908
LC78625E
DSP
EFM Decode
LD DATA
56
IC352
CA0002AM
Analog Audio
25
4
15
14
Analog L
Analog R
Phillips Code
ACOM
IC400
LA7134M
VDEM
27
10
37
IC500
PD6159B
Dual DVP
SPDL Cont
14-21
65-72
44-51
IC101
PD3212A
Memory Cont. (with DNR)
IC102, IC103
MB81C1501PF
Field Memory
14M VCXO


IC802
MB811171622A
-100FN
16Mbit SDRAM
CODE Buffer
(Video, Audio, Sub-picture,GUI)
IC 801
MB86371
Memory Controller
CPU
I/F
System
Decoder
(DMUX)
MPEG 2
Video
Decoder
Sub
Picture
Decoder
GUI
MIX
NTSC
/PAL
Encode
Copy Gurd
DAC
DAC
DAC
AV Sync
Controller
AC3/MPEG1
Audio Decoder
S/PDIF
DVD/V-CD
AV Decoder
27M
36M
DVD Y
(IC815 ①)
Sync Tip
Clamp
(from MECHA. CONT. ㊶)
D-EXT ON/OFF
LD Y SIGNAL
(from MYCB)
AMP
D-Extention
Circuit
Pedestal
Clamp
Sync Tip
Clamp
LD Y
TRAP
IC620
Y OUT
C OUT
to
MYCB
BLANKING PLUSE
(from AV-1 ㊽)
BURST FLAG
(from AV-1 ㊼)
LD C SIGNAL
(from MYCB)
DVD C
(IC815 ⑦)
IC620
KEY
Front Section
FL
Cont.
FL TUBE
A.B.
Key
REMOTE
SENSOR
DATA
Hi-Bit
PCM Digital
PD
Key
DVD C.
DVD Y.
AC-3/PCM Digital
SEL IR
IR
X311
384 × 44.1k
(16M)
VCXO
Sel
IC203
TC74HC157AF
CLK
Hi-Bit
IC202
PD0236AM
D/A
L
R
Sel
Sel
IC201
PD2029AM (L)
16M
SR IN
SR OUT
L OUT
R OUT
JCKB ASSY
(COAXIAL)
(TOSLINK)
AC-3
/PCM
Digital
OUT
PCM
Digital OUT
AC-3 RF
AC-3 RF OUT
C (DVD)
Y (DVD)
IC301
CXD2046Q
Y/C SEP.
D/A
D/A
Y (LD)
C (LD)
1-8
IC620
IC620
TC74HC4053AF
Y OUT
C OUT
Comp. OUT
MYCB ASSY
CLDM ASSY

1.2 EXPLANATION OF EACH MOVEMENT

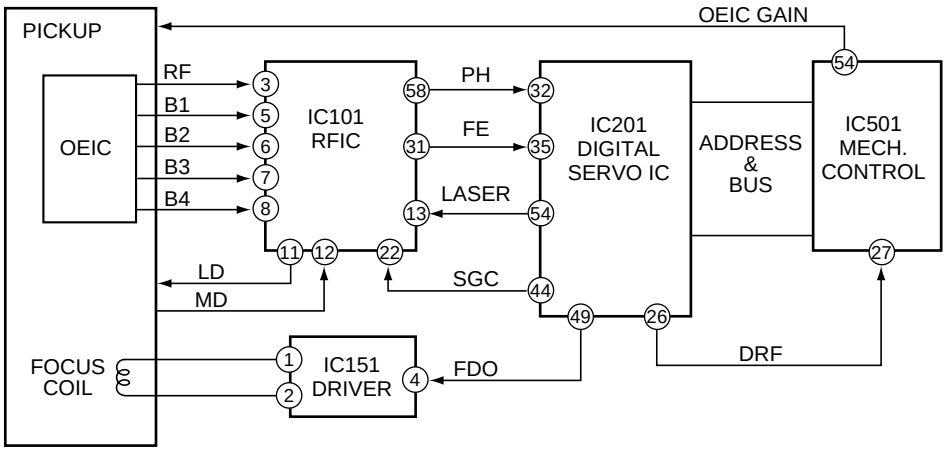
1.2.1 Sequence Up to Playback



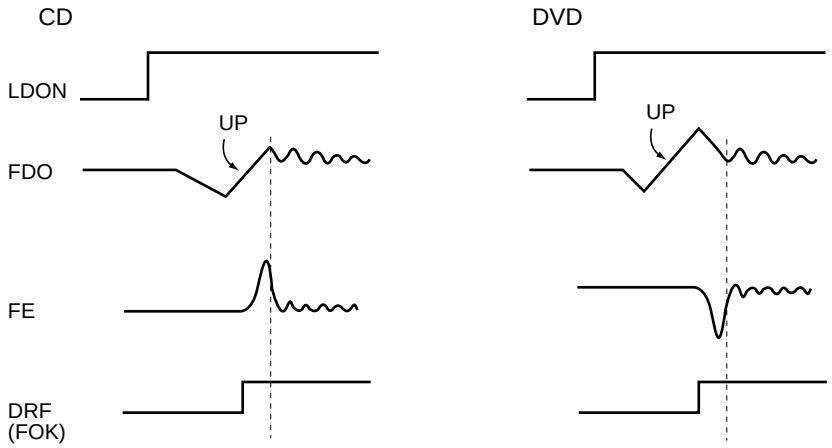
1.2.2 Focus Servo

FE generated in the RF IC is sent to the Digital servo IC.
For a DVD, the servo is turned on during the transition from "Up" to "Down" of the first-order sine wave. For a CD, it turns on during the transition from "Down" to "Up" of the first-order sine wave.
When the servo is turned on, the level of PH (the envelope of the bright side of RF) increases, and DRF becomes H. The kick-brake pulses, such as those for FOCUS jump, are also output from pin 49 of IC201.

• FOCUS SERVO



• FOCUS LOCK TIMING



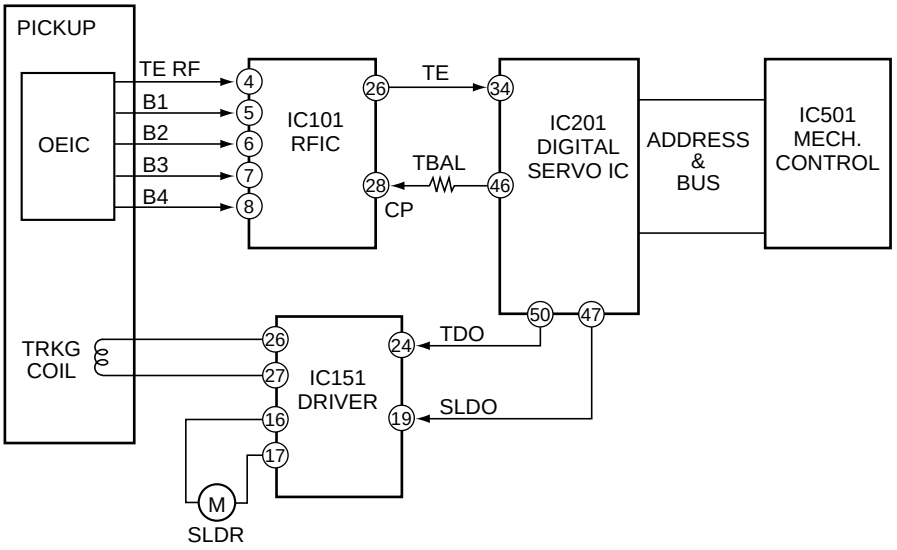
1.2.3 Tracking / Slider Servo

ATB: The tracking balance compensation is achieved by outputting the offset from the TBAL output at pin 46 of the digital servo IC, and by biasing the charge pump resistor for phase-difference error of RFIC.
The difference is detected by processing TE at pin 34 of IC 201 with an internal digital equalizer.

TDO: In addition to the servo output, the low-band components, such as the kick-brake for jump, are added for TDO output.

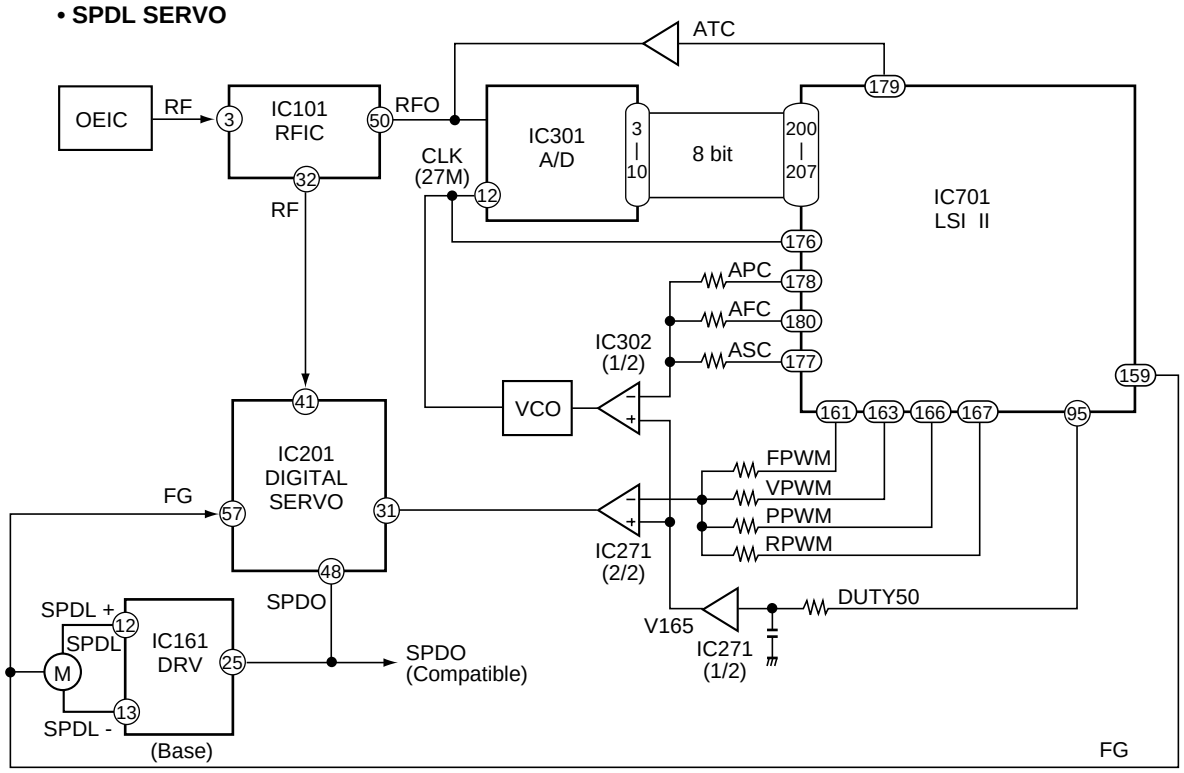
SLDO: The low-band components of TE are processed by the internal digital equalizer, and deadband is added for SLDO output. The offset voltage for pickup movement is also included in the SLDO output.

• TRACKING / SLIDER SERVO



1.2.4 SPINDLE SERVO

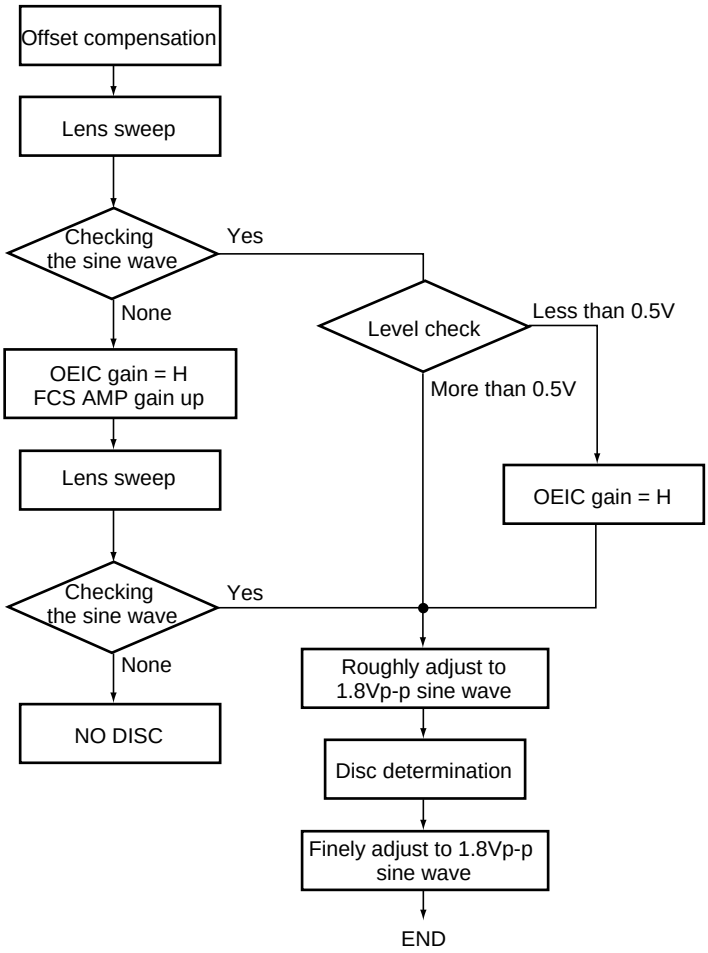
• SPDL SERVO



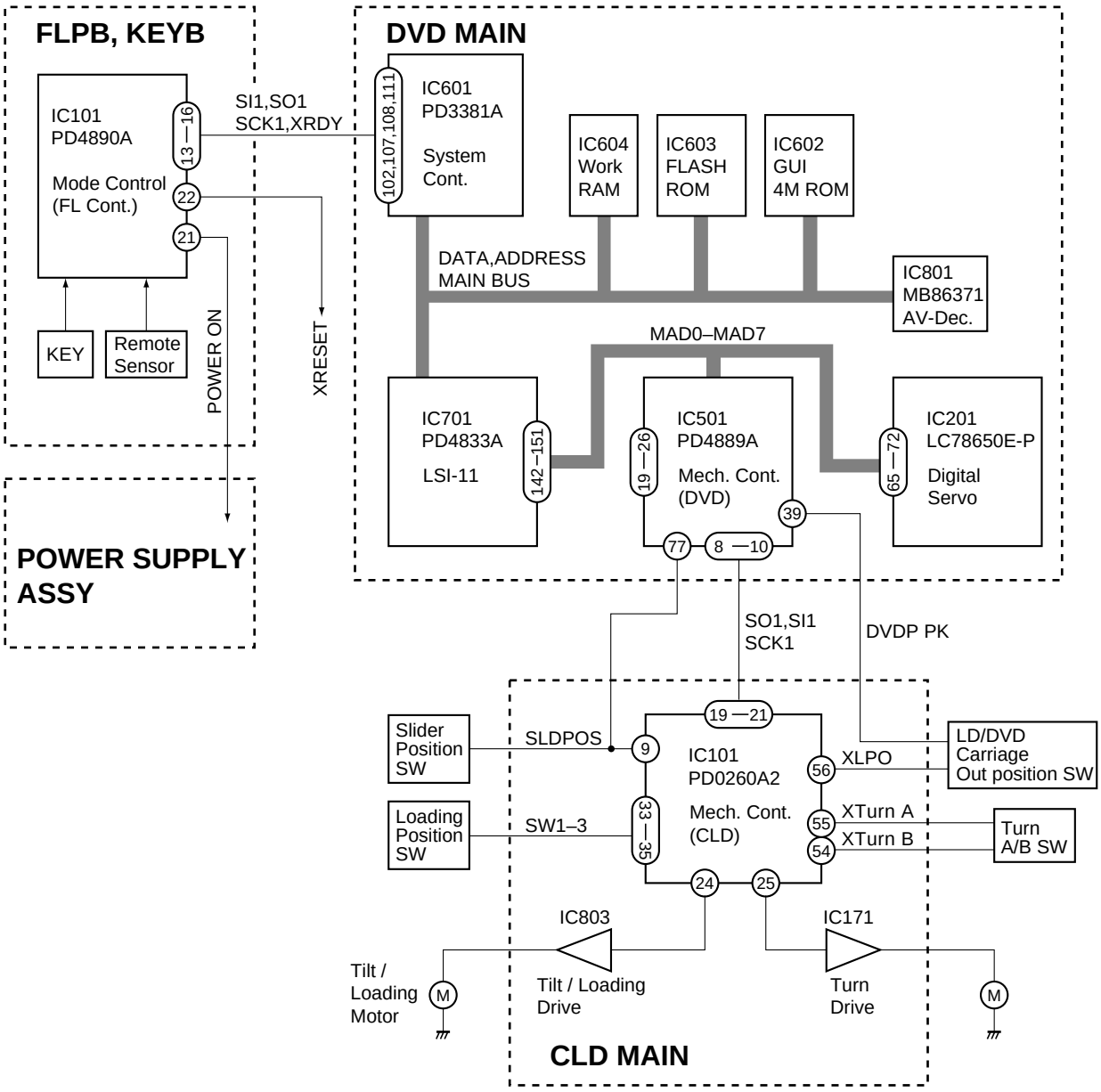
For a CD, the RF signal output from pin 32 of the RF IC is converted to binary in IC201. By comparing the binary value with the reference CLK (clock), the SPDL ERR signal is output from pin 48.
For a DVD, the SPDL ERR signal is generated from the PWM signal output from LSI-II. Upon receiving this signal via pin 31, IC201 also outputs it from pin 48, switching from the CD SPDL ERR signal.

1.2.5 Disc Determination

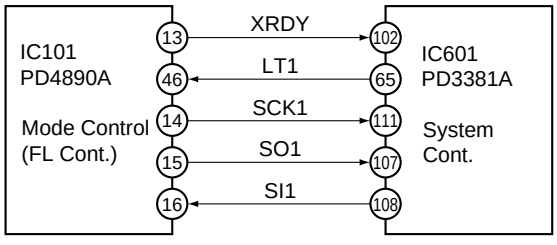
Determination is achieved by checking the sine wave by sweeping the lens with the OE IC gain at L and the FSC error amplifier (SGC) at the default setting. If no sine wave is detected, checking is retried after switching the OE IC gain to H and increasing the gain of the FSC error amplifier (SGC). If no sine wave is detected again, it is regarded as the NO DISC condition.
If one half of the sine wave detected at the first lens sweep is of a value less than 0.5 V, the OE IC gain is set to H and the peak-to-peak value of the sine wave is roughly adjusted to 1.8 Vp-p.
By sweeping the lens around the height where the sine wave has been detected, disc determination is performed, and the sine wave is finely adjusted to 1.8 Vp-p.

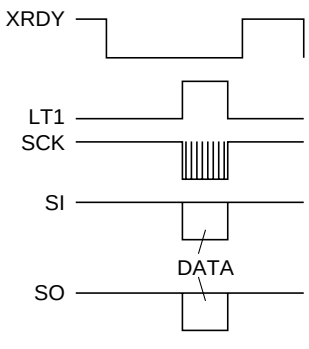


1.2.6 System Control (DVL-909)



1) Interface between Mode Cont. and System Cont.





Timing Chart

If there is no communication for 2 sec.,
Mode Cont. turn off the power and reset.