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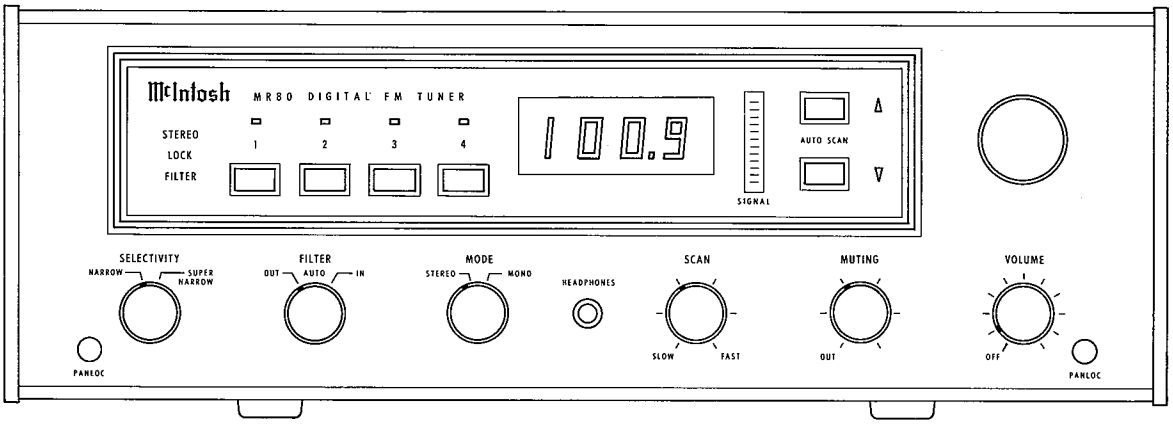
MR 80

DIGITAL FM TUNER



McIntosh

service manual

039215 Price $20.00

TABLE OF CONTENTS

GENERAL NOTES

1. Unless otherwise noted, all voltages indicated on the schematics are measured under the following conditions:

   a. AC input at 120 volts, 50 / 60Hz.

   b. Except for the regulated circuits in the power supply, all voltages are ±20% with respect to ground. A high impedance voltmeter must be used.

   c. No signal at antenna or cable input terminals.

   d. Front panel controls set at:
   SELECTIVITY ..... NARROW
   FILTER ..... OUT
   MODE ..... STEREO
   SCAN .....CCW or SLOW
   MUTING ..... OUT
   VOLUME .....ON

   e. Top panel controls set at:
   PRESELECTOR ..... OUT
   INPUT ..... ANT
   LOCK ..... ON
   DE-EMPHASIS....75μS & OUT
   SIGNAL STRENGTH....CCW

   f. Rear panel controls set at:
   STATIONS ..... PRESET

2. Unless otherwise specified:

   a. Resistance values are in ohms, 1/4 watt, 5% tolerance.

   b. Capacitance values smaller than 1 are in microfarads (μF), and capacitance values greater than 1 are in picofarads (pF).

   c. Inductors are in microhenries (μH).

3. When the MR 80 is connected to the 120V line voltage, but is not connected to any other device (preamp, power amp, antenna, test equipment, etc.), there is a chance the frequency display will blank out when tuning with the main tuning knob. This is normal and can easily be corrected by reversing the 120V AC line plug, or by connecting the MR 80 to any other equipment.

4. Logic voltage levels:

   a. All logic is positive. The most positive voltage level is a logic high or 1.

   b. The symbol for B-series CMOS is a double quotation mark:
   "0" or logic low (−.32V to +4V)
   "1" or logic high (+11.9V to +15.3V)

   c. The symbol for TTL and low power Schottky is a single quotation mark:
   '0' or logic low (−.7V to +.8V)
   '1' or logic high (+2V to +5V)

   d. The symbol for ECL is a double dash line:
   -0- or logic low (−1.475V to −1.85V)
   -1- or logic high (−1.105V to −0.81V)

5. Logic Truth Tables: Refer to page 13-3

6. Many of the semiconductor devices (CMOS and NMOS) used in the MR 80 are inherently sensitive to static electricity when not connected to a circuit, and can be permanently damaged by a static electricity discharge. When these devices are removed from a circuit, they should have their leads embedded in conductive-carbon foam or aluminum foil to protect them. Follow the removal and installation procedures below to insure against static electricity damage.

   TO REMOVE:

   a. Turn power off to the MR 80.

   b. Touch one hand to the chassis, then remove the semiconductor from the circuit with the other hand.

   c. Touch one hand to the conductive-carbon foam (or aluminum foil), then embed the leads of the semiconductor in the foam with the other hand.

   TO INSTALL:

   a. Turn power off to the MR 80.

   b. Touch one hand to the conductive foam (or aluminum foil), then remove the semiconductor from the foam with the other hand.

   c. Touch one hand to the chassis, then install the semiconductor in the circuit.

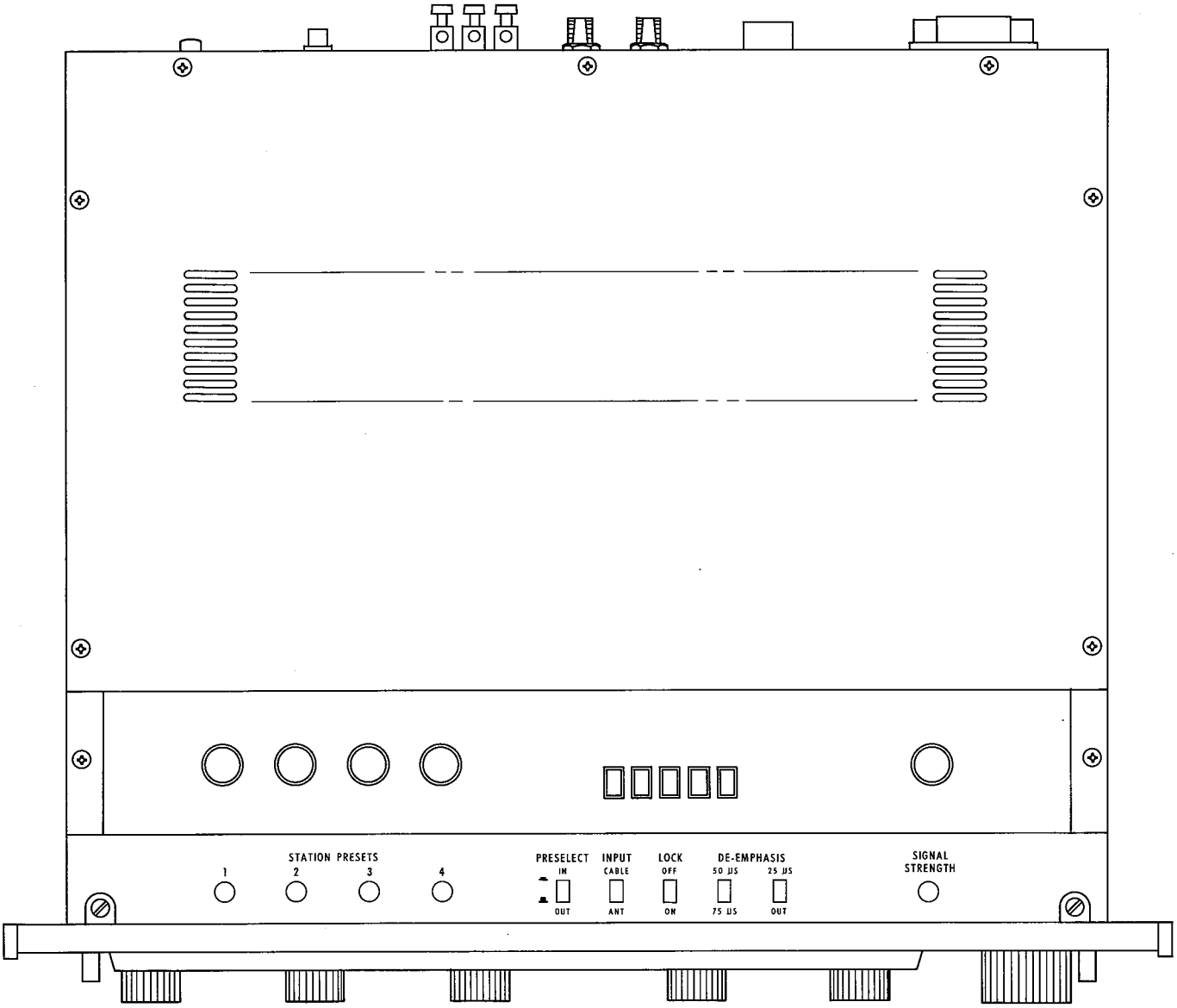


Fig. 0-1. TOP VIEW

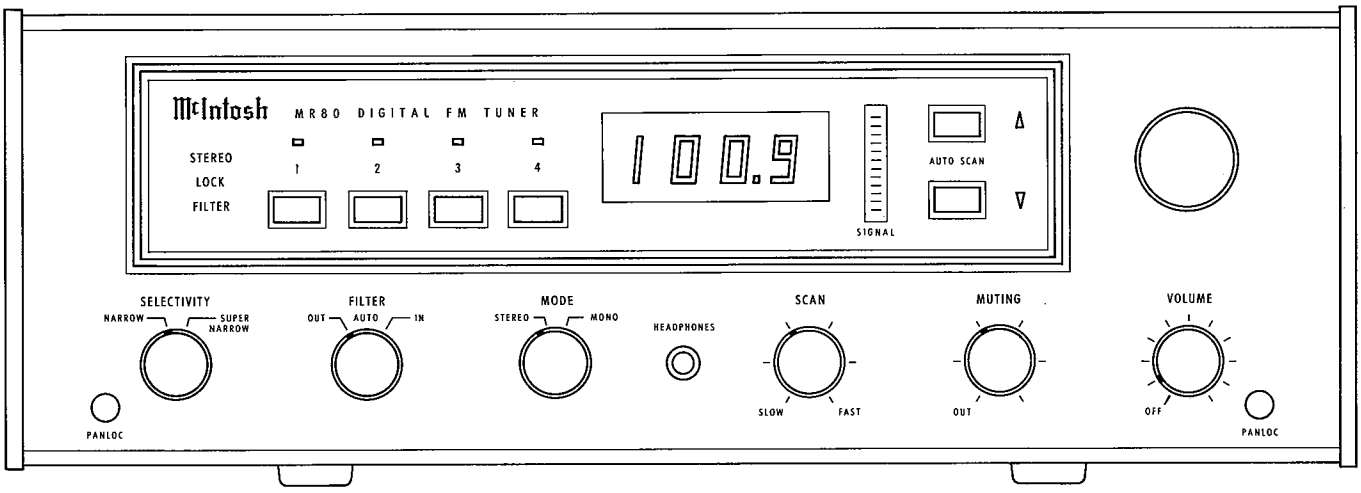


Fig. 0-2. FRONT VIEW

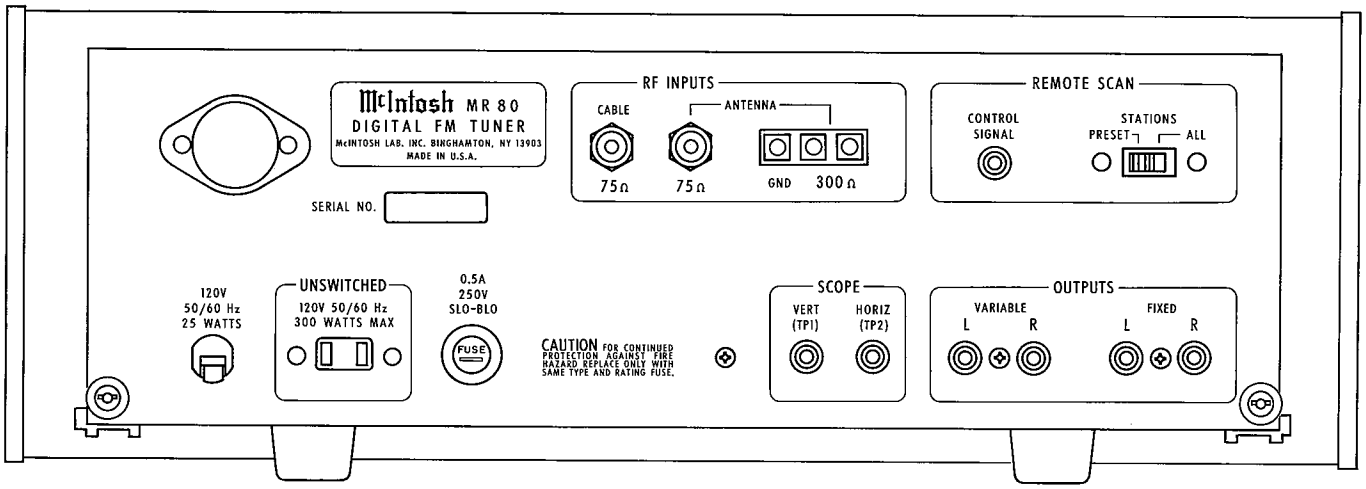


Fig. 0-3. REAR VIEW

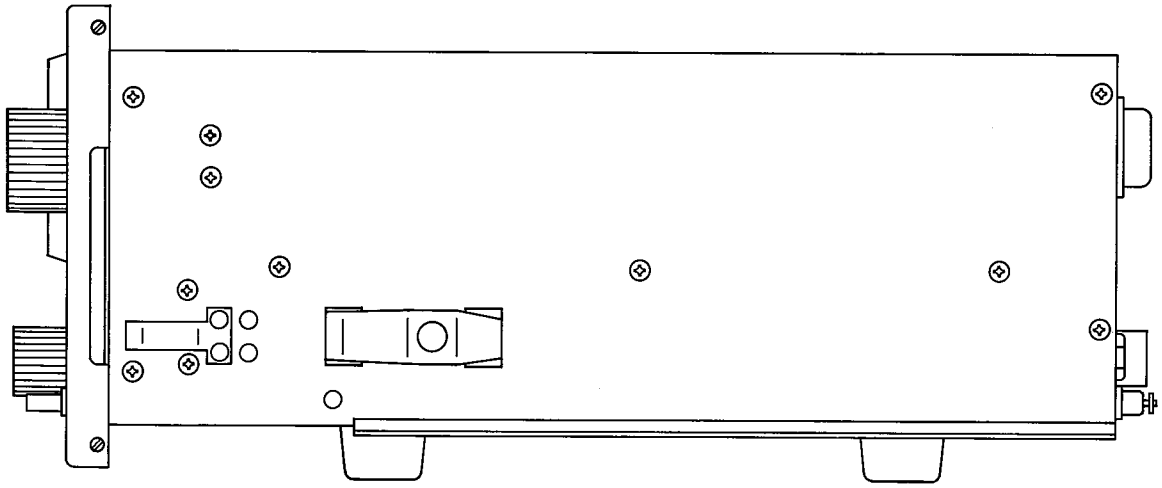


Fig. 0-4. SIDE VIEW

SYMBOL DESIGNATIONS

1. The heavy lines on the schematics denote the primary signal path.

2. The terminal numbering of rotary switches is for reference only. A dot on the rotor of a rotary switch indicates there is an electrical connection between the front and rear rotor section.

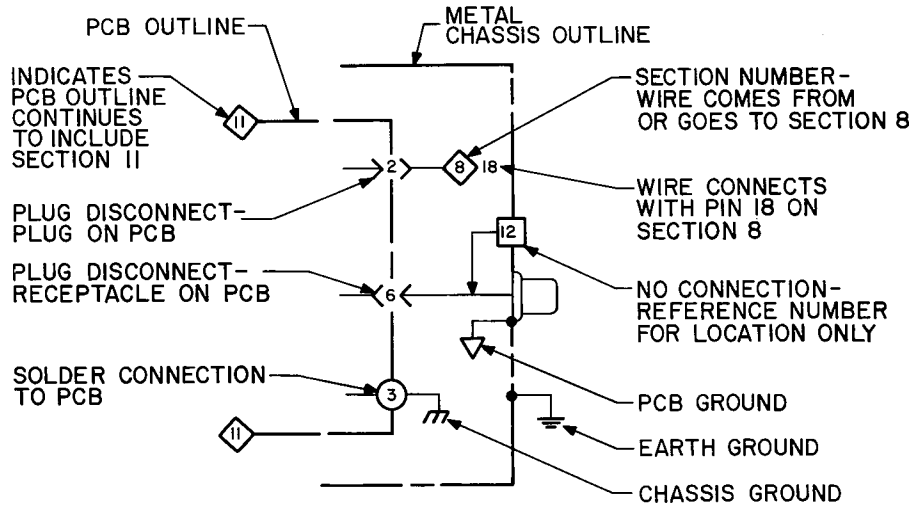
3. Letter designations for symbol numbers:
   - C - Capacitors
   - CB - Circuit Breaker
   - D - Diodes
   - DS - Lamps and Lighting Devices
   - E - Ferrite Beads
   - F - Fuses
   - FN - Filters
   - IC - Integrated Circuits
   - J - Jack
   - K - Relay
   - L - Inductors, Coils and Chokes
   - LDR - Light Dependent Resistors
   - M - Meters
   - Q - Transistors
   - R - Resistors and Potentiometers
   - RT - Thermistors
   - S - Switches
   - T - Transformers
   - Y - Crystals

4. A "D" between the collector and emitter of a transistor symbol on the circuit side of a PCB layout identifies the transistor as a Darlington transistor.

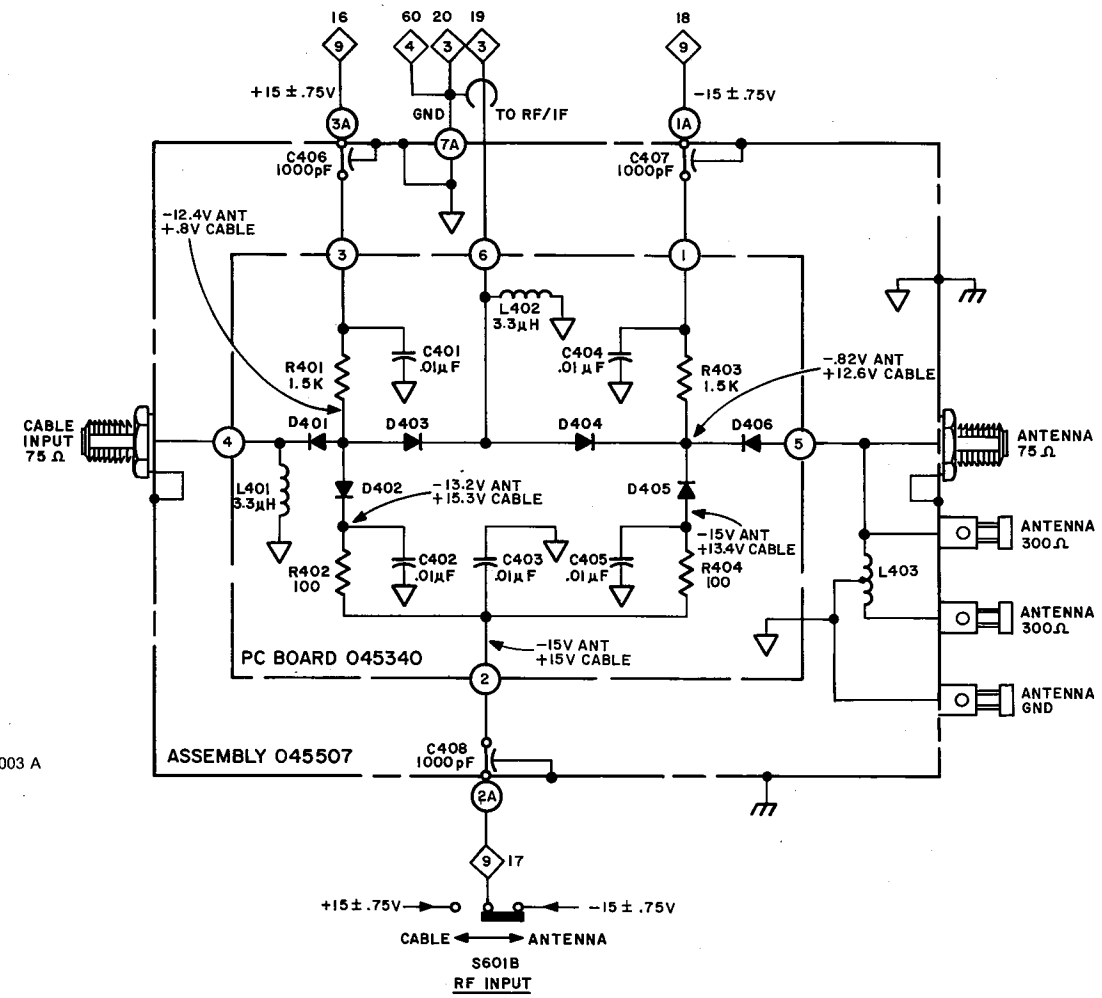
5. Marking to identify location of controls:

MUTING	Front panel
(MUTING)	Rear panel
MUTING	Top panel

6. All schematic symbols used in this manual are in conformance with the book, "Electrical and Electronics Graphic Symbols and Reference Designations" published by the Institute of Electrical and Electronics Engineers. (IEEE Std 315-1975, ANSI Y32.2-1975, and CSA Z99-1975)



ANTENNA SWITCH ASSEMBLY

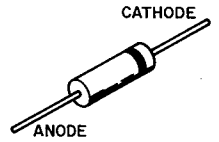


Schematic No. 156003 A

SECTION 2 NOTES

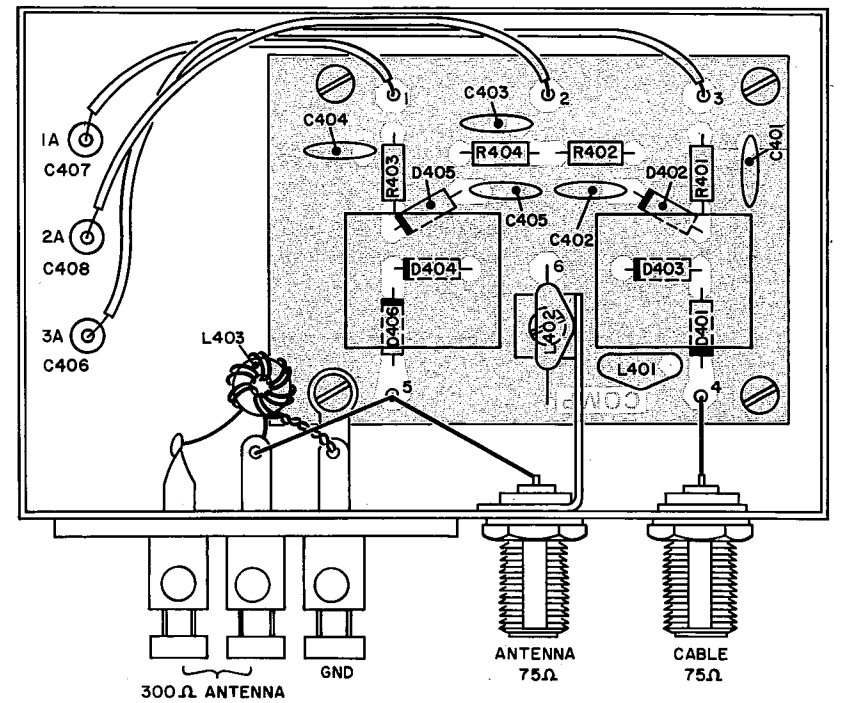
Diodes D401 through D406 are PIN Diodes. DO NOT SUBSTITUTE as performance may be affected

SEMICONDUCTOR IDENTIFICATION



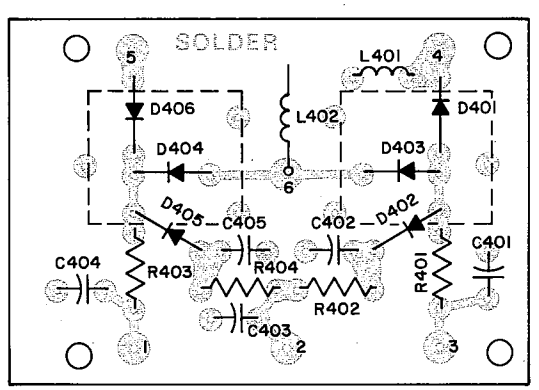
D401-D406

COMPONENT SIDE



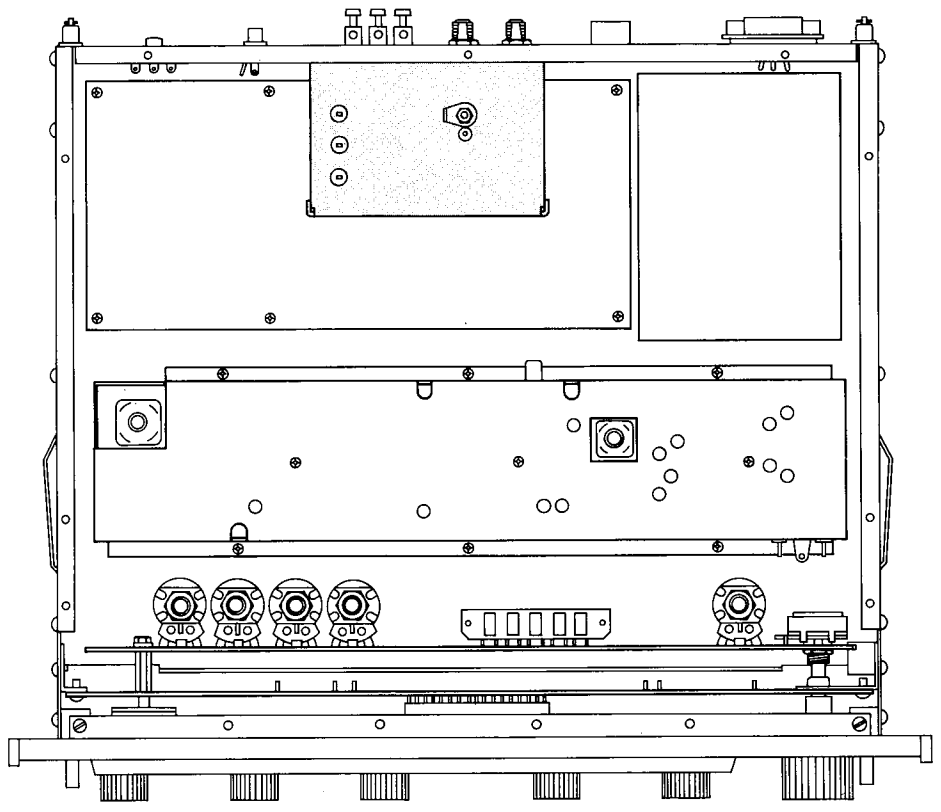
PC BOARD 045340

CIRCUIT SIDE



Section 2

ANTENNA SWITCH ASSEMBLY



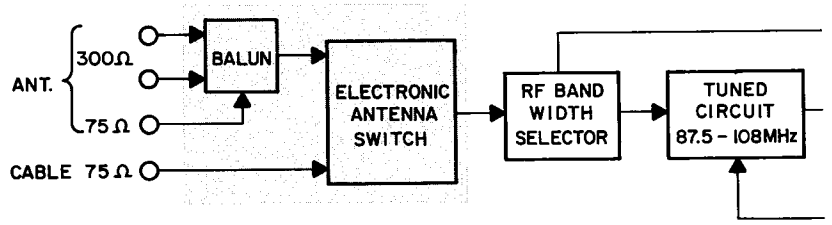
SECTION LOCATION - TOP VIEW

SECTION 2 PARTS LIST

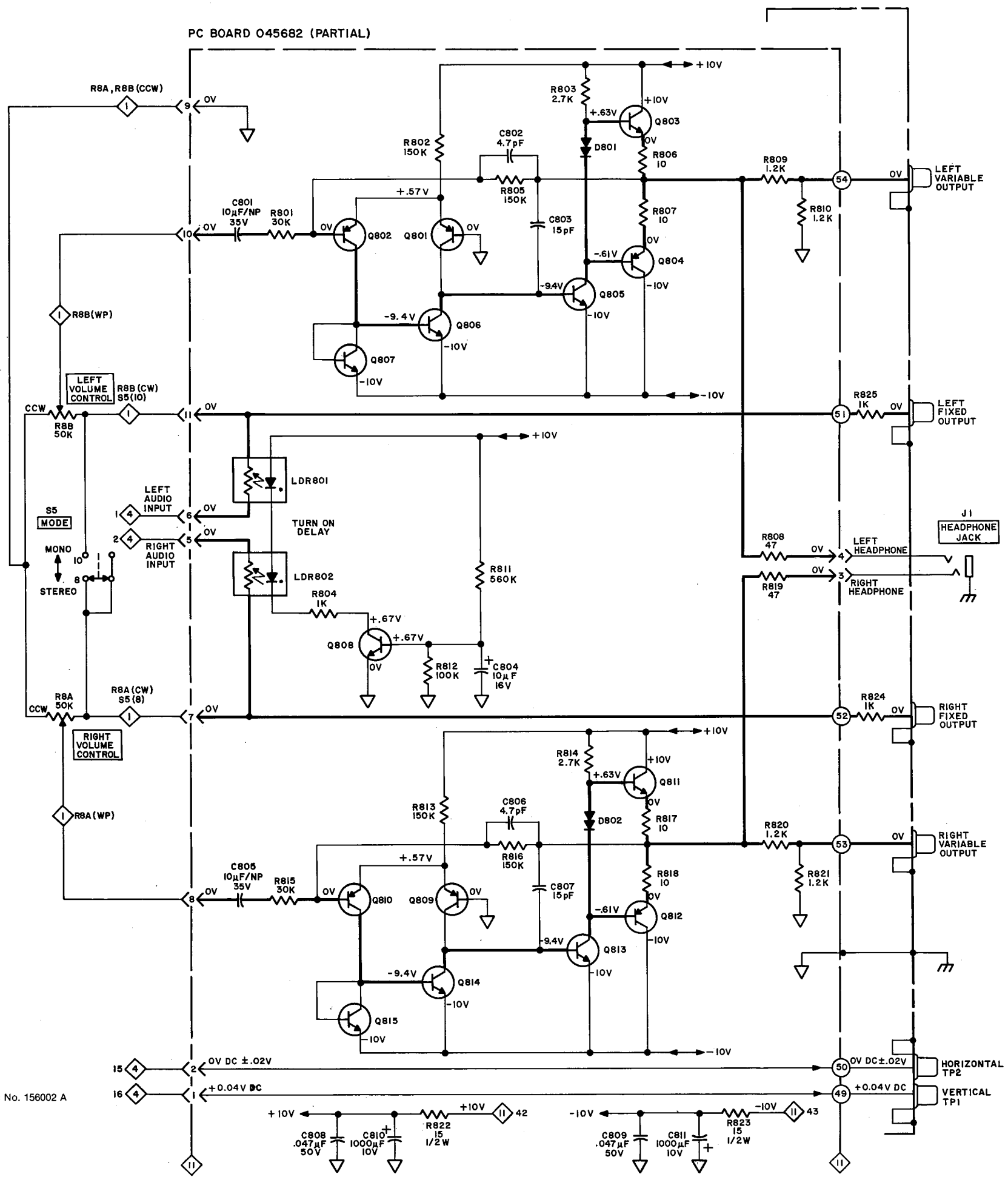
Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
CAPACITORS (CD = Ceramic Disc)				
C401	061159	CD, .01μF, +80 – 20%, 50V		
C402	061159	CD, .01μF, +80 – 20%, 50V		
C403	061159	CD, .01μF, +80 – 20%, 50V		
C404	061159	CD, .01μF, +80 – 20%, 50V		
C405	061159	CD, .01μF, +80 – 20%, 50V		
*C406	061101	Feed-Thru, 1000pF, GMV		
*C407	061101	Feed-Thru, 1000pF, GMV		
*C408	061101	Feed-Thru, 1000pF, GMV		
DIODES				
*D401	070086	Pin Diode, 35V, HP5082-3188		
*D402	070086	Pin Diode, 35V, HP5082-3188		
*D403	070086	Pin Diode, 35V, HP5082-3188		
*D404	070086	Pin Diode, 35V, HP5082-3188		
*D405	070086	Pin Diode, 35V, HP5082-3188		
*D406	070086	Pin Diode, 35V, HP5082-3188		
INDUCTORS/COILS				
*L401	122184	3.3μH, Coil		
*L402	122184	3.3μH, Coil		
*L403	045267	Balun		
RESISTORS (CF = Carbon Film)				
R401	141053	CF, 1.5K, 5%, 1/4W		
R402	141025	CF, 100, 5%, 1/4W		
R403	141053	CF, 1.5K, 5%, 1/4W		
R404	141025	CF, 100, 5%, 1/4W		
MISCELLANEOUS				
	*074033	Push Terminal		
	*117234	Coax Receptacle		

*Parts marked with an asterisk (*) are replacement parts stocked by our Service Department and can be ordered only by part number from McIntosh. Parts not marked can be obtained from electronic parts suppliers.

BLOCK DIAGRAM



HEADPHONE AMPLIFIER and TURN-ON DELAY



Schematic No. 156002 A

Section 5

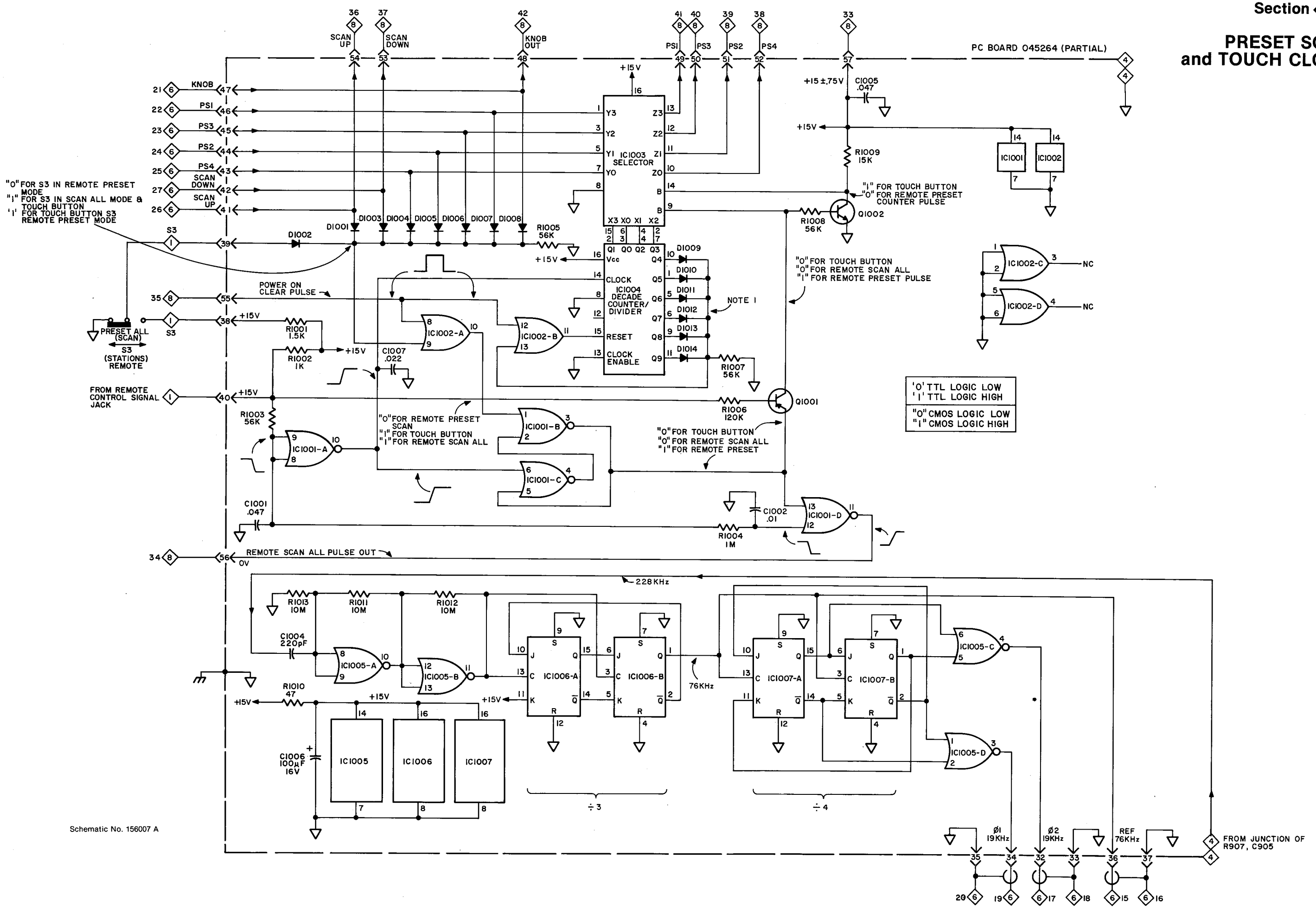
HEADPHONE AMPLIFIER and TURN-ON DELAY

SECTION 5 PARTS LIST

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
CAPACITORS (Elect = Electrolytic, CD = Ceramic Disc)				
C801	066173	Elect, 10μF, NP, 35V		
C802	061004	CD, 4.7pF, 10%, NPO		
C803	061011	CD, 15pF, 10%, NPO		
C804	066211	Elect, 10μF, 16V		
C805	066173	Elect, 10μF, NP, 35V		
C806	061004	CD, 4.7pF, 10%, NPO		
C807	061011	CD, 15pF, 10%, NPO		
C808	061161	CD, .047μF, +80−20%, 50V		
C809	061161	CD, .047μF, +80−20%, 50V		
C810	066309	Elect, 1000μF, 10V		
C811	066309	Elect, 1000μF, 10V		
DIODES				
*D801	070046	Silicon, Stabistor, 1.344V, 2%@10mA, IN816		
*D802	070046	Silicon, Stabistor, 1.344V, 2%@10mA, IN816		
LIGHT DEPENDENT RESISTORS				
*LDR801	144070	LDR		
*LDR802	144070	LDR		
TRANSISTORS				
*Q801	132056	Silicon, PNP, 2N5087		
*Q802	132056	Silicon, PNP, 2N5087		
*Q803	132171	Silicon, NPN, MPS-A05		
*Q804	132172	Silicon, PNP, MPS-A55		
*Q805	132185	Silicon, NPN, 2N6429A		
*Q806	132143	Silicon, NPN, MPS-D05		
*Q807	132143	Silicon, NPN, MPS-D05		
*Q808	132185	Silicon, NPN, 2N6429A		
*Q809	132056	Silicon, PNP, 2N5087		
*Q810	132056	Silicon, PNP, 2N5087		
*Q811	132171	Silicon, NPN, MPS-A05		
*Q812	132172	Silicon, PNP, MPS-A55		
*Q813	132185	Silicon, NPN, 2N6429A		
*Q814	132143	Silicon, NPN, MPS-D05		
*Q815	132143	Silicon, NPN, MPS-D05		

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
RESISTORS (CC = Carbon Composition, CF = Carbon Film)				
R801	141083	CF, 30K, 5%, 1/4W		
R802	141100	CF, 150K, 5%, 1/4W		
R803	141059	CF, 2.7K, 5%, 1/4W		
R804	141049	CF, 1K, 5%, 1/4W		
R805	141100	CF, 150K, 5%, 1/4W		
R806	141136	CF, 10, 5%, 1/4W		
R807	141136	CF, 10, 5%, 1/4W		
R808	141152	CF, 47, 5%, 1/4W		
R809	141051	CF, 1.2K, 5%, 1/4W		
R810	141051	CF, 1.2K, 5%, 1/4W		
R811	141114	CF, 560K, 5%, 1/4W		
R812	141096	CF, 100K, 5%, 1/4W		
R813	141100	CF, 150K, 5%, 1/4W		
R814	141059	CF, 2.7K, 5%, 1/4W		
R815	141083	CF, 30K, 5%, 1/4W		
R816	141100	CF, 150K, 5%, 1/4W		
R817	141136	CF, 10, 5%, 1/4W		
R818	141136	CF, 10, 5%, 1/4W		
R819	141152	CF, 47, 5%, 1/4W		
R820	141051	CF, 1.2K, 5%, 1/4W		
R821	141051	CF, 1.2K, 5%, 1/4W		
R822	136033	CC, 15, 10%, 1/2W		
R823	136033	CC, 15, 10%, 1/2W		
R824	141049	CF, 1K, 5%, 1/4W		
R825	141049	CF, 1K, 5%, 1/4W		
MISCELLANEOUS				
	045480	Bracket W/Jacks		

*Parts marked with an asterisk (*) are replacement parts stocked by our Service Department and can be ordered only by part number from McIntosh. Parts not marked can be obtained from electronic parts suppliers.



Schematic No. 156007 A

Section 7

PRESET SCAN and TOUCH CLOCK

SECTION 7 PARTS LIST

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
CAPACITORS (Elect = Electrolytic, MPE = Metalized Polyester, CD = Ceramic Disc)				
C1001	061161	CD, .047μF, +80 – 20%, 50V		
C1002	061159	CD, .01μF, +80 – 20%, 50V		
C1003		Not Used		
C1004	061028	CD, 220pF, 20%		
C1005	061161	CD, .047μF, +80 – 20%, 50V		
C1006	066226	Elect, 100μF, 16V		
*C1007	064178	MPE, .022μF, 5%, 63V		
DIODES				
*D1001	070047	Silicon, 1N4148		
*D1002	070047	Silicon, 1N4148		
*D1003	070047	Silicon, 1N4148		
*D1004	070047	Silicon, 1N4148		
*D1005	070047	Silicon, 1N4148		
*D1006	070047	Silicon, 1N4148		
*D1007	070047	Silicon, 1N4148		
*D1008	070047	Silicon, 1N4148		
*D1009	070047	Silicon, 1N4148		
*D1010	070047	Silicon, 1N4148		
*D1011	070047	Silicon, 1N4148		
*D1012	070047	Silicon, 1N4148		
*D1013	070047	Silicon, 1N4148		
*D1014	070047	Silicon, 1N4148		
INTEGRATED CIRCUITS				
*IC1001	133064	CMOS Quad 2-Input "Nor" Gate, CD4001B		
*IC1002	133073	CMOS Quad 2-Input "Or" Gate, CD4071B		
*IC1003	133083	Quad 2-Channel Data Selector, CD4519B, CMOS		
*IC1004	133084	Johnson Decade Counter, CD4017B, CMOS		
*IC1005	133064	CMOS Quad 2-Input "Nor" Gate, CD4001B		
*IC1006	133085	CMOS Dual J-K Flip-Flop, CD4027B		
*IC1007	133085	CMOS Dual J-K Flip-Flop, CD4027B		

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
TRANSISTORS				
*Q1001	132096	Sliicon, PNP, BC416C		
*Q1002	132143	Silicon, NPN, MPSD05		
RESISTORS (CF = Carbon Film)				
R1001	141053	CF, 1.5K, 5%, 1/4W		
R1002	141049	CF, 1K, 5%, 1/4W		
R1003	141090	CF, 56K, 5%, 1/4W		
R1004	141120	CF, 1M, 5%, 1/4W		
R1005	141090	CF, 56K, 5%, 1/4W		
R1006	141098	CF, 120K, 5%, 1/4W		
R1007	141090	CF, 56K, 5%, 1/4W		
R1008	141090	CF, 56K, 5%, 1/4W		
R1009	141076	CF, 15K 5%, 1/4W		
R1010	141152	CF, 47, 5%, 1/4W		
R1011	141132	CF, 10M, 5%, 1/4W		
R1012	141132	CF, 10M, 5%, 1/4W		
R1013	141132	CF, 10M, 5%, 1/4W		

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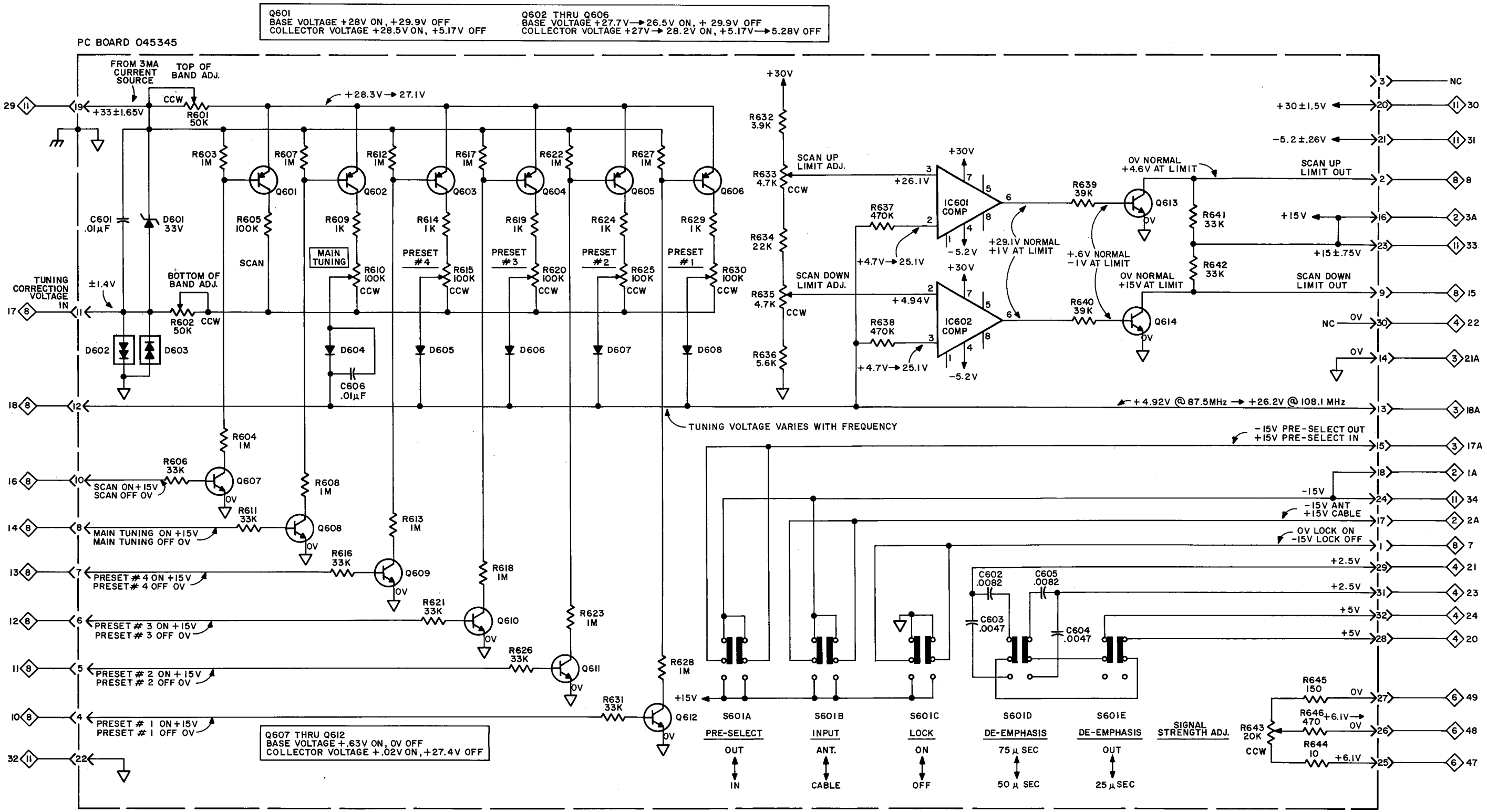
TOP COVER CONTROLS, BAND LIMITS, MAIN TUNING and PRESET TUNING



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Section 9

TOP COVER CONTROLS, BAND LIMITS, MAIN TUNING and PRESET TUNING

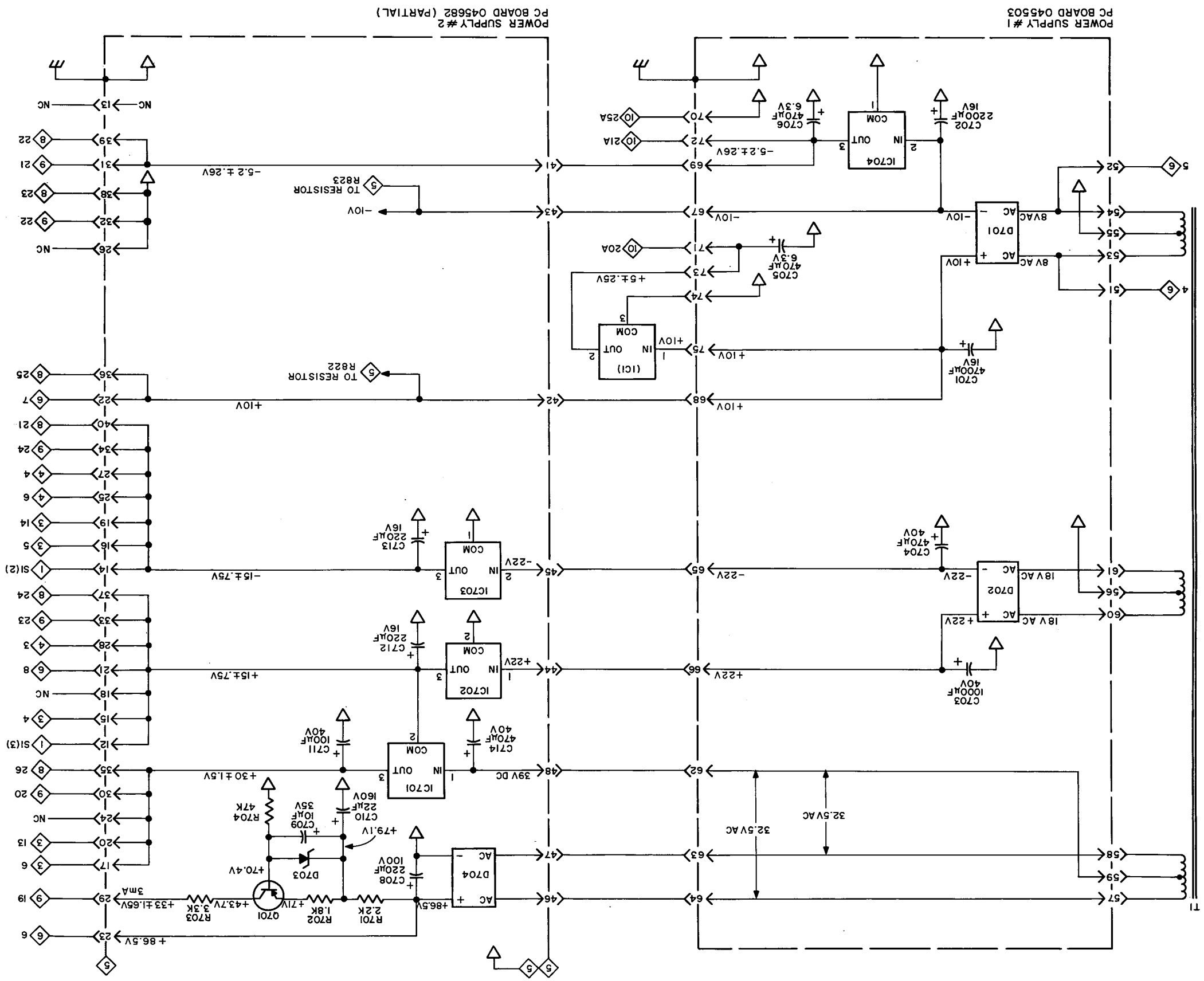
SECTION 9 PARTS LIST

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
CAPACITORS (PF = Polyester Film, CD = Ceramic Disc)				
C601	061159	CD, .01μF, +80-20%, 50V		
*C602	064172	PF, .0082μF, 5%, 100V		
*C603	064169	PF, .0047μF, 5%, 100V		
*C604	064169	PF, .0047μF, 5%, 100V		
*C605	064172	PF, .0082μF, 5%, 100V		
C606	061159	CD, .01μF, +80-20%, 50V		
DIODES				
*D601	070113	Zener, 33V, MVS460		
*D602	070046	Silicon, Stabistor, 1.344V, 2%, 10mA, MZ2361		
*D603	070046	Silicon, Stabistor, 1.344V, 2%, 10mA, MZ2361		
*D604	070098	Silicon, 400mW, FDH400		
*D605	070098	Silicon, 400mW, FDH400		
*D606	070098	Silicon, 400mW, FDH400		
*D607	070098	Silicon, 400mW, FDH400		
*D608	070098	Silicon, 400mW, FDH400		
INTEGRATED CIRCUITS				
*IC601	133043	Op Amp, LF-356-1M		
*IC602	133043	Op Amp, LF-356-1M		
TRANSISTORS				
*Q601	132136	Silicon, PNP, MPSA93		
*Q602	132136	Silicon, PNP, MPSA93		
*Q603	132136	Silicon, PNP, MPSA93		
*Q604	132136	Silicon, PNP, MPSA93		
*Q605	132136	Silicon, PNP, MPSA93		
*Q606	132136	Silicon, PNP, MPSA93		
*Q607	132147	Silicon, NPN, MPSA42		
*Q608	132147	Silicon, NPN, MPSA42		
*Q609	132147	Silicon, NPN, MPSA42		
*Q610	132147	Silicon, NPN, MPSA42		
*Q611	132147	Silicon, NPN, MPSA42		
*Q612	132147	Silicon, NPN, MPSA42		
*Q613	132171	Silicon, NPN, MPSA05		
*Q614	132171	Silicon, NPN, MPSA05		

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
RESISTORS (CF = Carbon Film, Pot = Potentiometer)				
*R601	134375	Pot, 50K Trim		
*R602	134375	Pot, 50K Trim		
R603	141120	CF, 1M, 5%, 1/4W		
R604	141120	CF, 1M, 5%, 1/4W		
R605	141096	CF, 100K, 5%, 1/4W		
R606	141084	CF, 33K, 5%, 1/4W		
R607	141120	CF, 1M, 5%, 1/4W		
R608	141120	CF, 1M, 5%, 1/4W		
R609	141049	CF, 1K, 5%, 1/4W		
*R610	134376	Pot, 100K, Tuning Control		
R611	141084	CF, 33K, 5%, 1/4W		
R612	141120	CF, 1M, 5%, 1/4W		
R613	141120	CF, 1M, 5%, 1/4W		
R614	141049	CF, 1K, 5%, 1/4W		
*R615	134374	Pot, 100K, Preset		
R616	141084	CF, 33K, 5%, 1/4W		
R617	141120	CF, 1M, 5%, 1/4W		
R618	141120	CF, 1M, 5%, 1/4W		
R619	141049	CF, 1K, 5%, 1/4W		
*R620	134374	Pot, 100K, Preset		
R621	141084	CF, 33K, 5%, 1/4W		
R622	141120	CF, 1M, 5%, 1/4W		
R623	141120	CF, 1M, 5%, 1/4W		
R624	141049	CF, 1K, 5%, 1/4W		
*R625	134374	Pot, 100K, Preset		
R626	141084	CF, 33K, 5%, 1/4W		
R627	141120	CF, 1M, 5%, 1/4W		
R628	141120	CF, 1M, 5%, 1/4W		
R629	141049	CF, 1K, 5%, 1/4W		
*R630	134374	Pot, 100K, Preset		
R631	141084	CF, 33K, 5%, 1/4W		
R632	141062	CF, 3.9K, 5%, 1/4W		
*R633	134307	Pot, 4.7K Trim		
R634	141080	CF, 22K, 5%, 1/4W		
*R635	134307	Pot, 4.7K Trim		
R636	141066	CF, 5.6K, 5%, 1/4W		
R637	141112	CF, 470K, 5%, 1/4W		
R638	141112	CF, 470K, 5%, 1/4W		
R639	141086	CF, 39K, 5%, 1/4W		
R640	141086	CF, 39K, 5%, 1/4W		
R641	141084	CF, 33K, 5%, 1/4W		
R642	141084	CF, 33K, 5%, 1/4W		
*R643	134373	Pot, 20K, Signal Strength		
R644	141136	CF, 10, 5%, 1/4W		
R645	141029	CF, 150, 5%, 1/4W		
SWITCHES				
*S601	150032	Pushbutton, DPDT, 5 Position		

*Parts marked with an asterisk (*) are replacement parts stocked by our Service Department and can be ordered only by part number from McIntosh. Parts not marked can be obtained from electronic parts suppliers.

Schematic No. 156005 A



POWER SUPPLY

SECTION 11 PARTS LIST

Symbol No.	Part No.	Name/Description	Serial No.	Ref. No.
CAPACITORS (Elect = Electrolytic,)				
C701	066324	Elect, 4700μF, 16V		
C702	066247	Elect, 2200μF, 16V		
C703	066323	Elect, 1000μF, 40V		
C704	066134	Elect, 470μF, 40V		
C705	066236	Elect, 470μF, 6.3V		
C706	066236	Elect, 470μF, 6.3V		
C707		Not Used		
C708	066245	Elect, 220μF, 100V		
C709	066239	Elect, 10μF, 35V		
C710	066303	Elect, 22μF, 160V		
C711	066206	Elect, 100μF, 40V		
C712	066218	Elect, 220μF, 16VDC		
C713	066218	Elect, 220μF, 16VDC		
C714	066134	Elect, 470μF, 40V		
DIODES				
*D701	070051	Silicon, Bridge, 50V, 4A, PE05		
*D702	070044	Silicon, Bridge, 400VRMS, 2A, PD40		
*D703	070085	Zener, 6.2V, 5%, 500mW, IN5234B		
*D704	070044	Silicon, Bridge, 400VRMS, 2A, PD40		
INTEGRATED CIRCUITS				
*IC701	133086	+ 15V Regulator, 7815CT, Assemble with Insulator 084099 & Shoulder Washer 104101		
*IC702	133086	+ 15V Regulator, 7815CT Assemble with Insulator 084099 & Shoulder Washer 104101		
*IC703	133087	− 15V Regulator, 7915CT, Assemble with Insulator 084099 & Shoulder Washer 104101		
*IC704	133088	-5.2V Regulator, MC7905.2CT, Assemble with Insulator 084099 & Shoulder Washer 104101		
TRANSISTORS				
*Q701	132148	Silicon, PNP, MPS-U57		
RESISTORS (CC = Carbon Composition, CF = Carbon Film)				
R701	141057	CF, 2.2K, 5%, 1/4W		
R702	141055	CF, 1.8K, 5%, 1/4W		
R703	141060	CF, 3.3K, 5%, 1/4W		
R704	141088	CF, 47K, 5%, 1/4W		

* Parts marked with an asterisk (*) are replacement parts stocked by our Service Department and can be ordered only by part number from McIntosh. Parts not marked can be obtained from electronic parts suppliers.

ALIGNMENT PROCEDURE

The alignment procedure below should not be started until the MR 80 and the test equipment have been turned on for a fifteen minute warm-up period. If the tuner is completely out of alignment, or an unauthorized alignment has been attempted, start with the Prealignment Procedure on the opposite page. Connect the MR 80 to the test equipment as shown on Page 12-3.

Set the front panel controls to the following positions:

SELECTIVITY.....NARROW
FILTER.....OUT
MODE.....STEREO
SCAN.....CCW or SLOW
MUTING.....OUT
VOLUME.....ON

Set the top cover controls to the following positions:

PRESELECT.....OUT
INPUT.....ANT
LOCK.....OFF
DE-EMPHASIS.....75μS & OUT
SIGNAL STRENGTH.....CCW

Set the rear panel controls to the following positions:

STATIONS.....PRESET

Remove the top rear cover, top control panel and bottom cover as described by the removal instructions on page 0-10. It is not necessary to remove the front panel.

A. **TOUCH CONTROL ADJUSTMENTS** (Section 6)

1. The front panel must be installed on the MR 80 for the adjustment of this section.

2. Tune STATION PRESET 2 to a known FM station. (NOTE: STATION PRESETS 1, 3, and 4, and the MAIN TUNING knob should not be tuned to the same station as PRESET 2.)

3. Using the variac, reduce the incoming AC voltage to the tuner from 120V AC to 90V AC.

4. Touch STATION PRESET 2 and adjust the TOUCH SENSITIVITY (R509-Section 6) so the indicating light for PRESET 2 comes on. The digital frequency display should show the correct frequency.

5. Using the variac, increase the incoming AC voltage from 90V AC to 120V AC.

6. Verify that all STATION PRESETS, SCAN UP, SCAN DOWN, and the MAIN TUNING knob are functioning.

B. **MAIN TUNING KNOB UPPER & LOWER TUNING BAND LIMITS** (Section 9)

1. Turn the MAIN TUNING knob CW until the digital display stops counting up, and then adjust TOP OF BAND LIMIT (R601—Section 9) for 108.1MHz display.

2. Turn the MAIN TUNING knob CCW until the digital display stops counting down, and then adjust BOTTOM OF BAND LIMIT (R602—Section 9) for 87.4MHz display.

3. Repeat Steps 1 and 2 until a correct digital display is accomplished. If not, see next step.

4. Check for correct tuning voltages with a voltmeter by connecting to Pin 18A on Section 3 PCB assembly. Using the MAIN TUNING knob, tune to 87.4MHz; you should measure +4.9V (±.05V), and at 108.1MHz you should measure +26.0V (±.25V). If the voltages are correct, proceed to SCAN UP AND DOWN BAND LIMITS (Step C). If either or both voltages are incorrect, proceed with Step 5 below.

5. If you did not obtain the correct voltages in Step 4, perform the following steps:
   a. Connect voltmeter to Pin 18A on Section 3 PCB assembly.
   b. Turn the slug in L211 (Section 3 PCB Assembly) 2 turns CW (starting with the slug flush with the top of coil form).
   c. Set C227 (Section 3 PCB) to fully closed (maximum capacitance).
   d. Turn the MAIN TUNING knob CW until the digital display stops counting up, and then adjust TOP OF BAND LIMIT (R601) for +26.0V (±.25V).
   e. Turn the MAIN TUNING knob CCW until the digital display stops counting down, and then adjust BOTTOM OF BAND LIMIT (R602) for +4.9V (±.05)
   f. Repeat Steps d. and e. until no further improvement is possible.
   g. Turn the MAIN TUNING knob CW until the digital display stops counting up, and then adjust C227 (Section 3) CCW for 108.1MHz.
   h. Turn the MAIN TUNING knob CCW until the digital display stops counting down, and then adjust L211 (Section 3) for 87.4MHz.
   i. Repeat Steps g. and h. until no further improvement is possible.

C. **SCAN UP AND DOWN BAND LIMITS** (Section 9)

1. Using the MAIN TUNING knob, tune to 90MHz.

2. Touch the SCAN DOWN touch button until the digital display stops counting down, and then, while maintaining finger contact, slowly adjust SCAN DOWN LIMIT (R635) until 87.4MHz is displayed.

3. Using the MAIN TUNING knob, tune to 107MHz.

4. Touch the SCAN UP touch button until the digital display stops counting up, and then, while maintaining finger contact, slowly adjust the SCAN UP LIMIT (R633) until 108.1MHz is displayed.

D. **RF, IF AND DETECTOR ALIGNMENT** (Section 3)

1. Using the MAIN TUNING knob, tune the MR 80 and the FM generator to 90.1MHz, or to a point of no interference either side of 90.1MHz. Set the generator for 1kμV (65 dBf), 100% modulation (±75kHz) at 1kHz mono.

2. With a scope connected to TP-1 and TP-2, tune the MR 80 so you can see the top of the IF curve.

3. Adjust the top slug of DETECTOR TRANSFORMER (T202—Section 3) for a centered horizontal multipath display.

4. Set up the distortion analyzer to measure distortion and then adjust the bottom slug of DETECTOR TRANSFORMER (T202—Section 3) for minimum distortion. See figure 12-1.

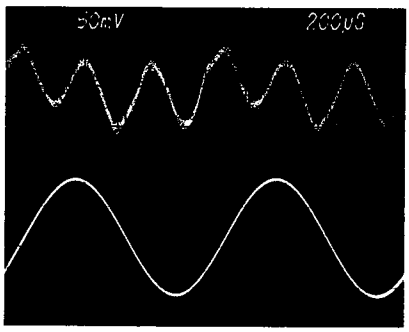


Figure 12-1. UPPER TRACE - distortion analyzer output. LOWER TRACE - tuner output going to distortion analyzer.

5. Switch LOCK (S601C—Section 9) to the ON position. Note: S601C will stay on throughout the remainder of the alignment.

6. Slowly adjust the bottom slug of DETECTOR TRANSFORMER (T202—Section 3) for minimum distortion.

7. Slowly adjust the top slug of DETECTOR TRANSFORMER (T202—Section 3) for minimum distortion.

8. Reduce the FM signal generator RF output level until the noise plus distortion increases to 3% THD or −30dB down (0dB = Set Level = 100% THD). Then on Section 3 PCB, adjust L204, L206, L207 and R224 MIXER BIAS ADJUST for maximum signal and minimum noise. See figures 12-2 & 12-3.

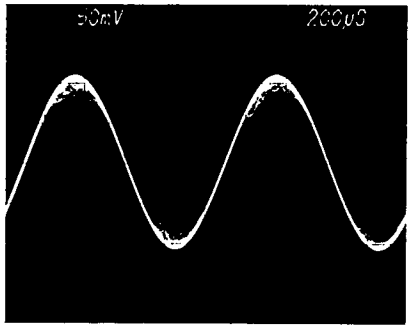


Figure 12-2. Tuner output going to distortion analyzer.

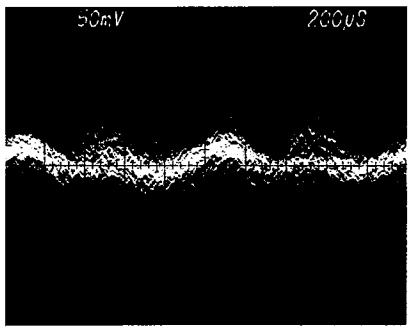


Figure 12-3. Distortion analyzer output.

9. Increase the FM signal generator RF output level to 100μV (45.5dBf), then switch PRESELECT (S601A—Section 9) to the IN position.

10. Reduce the FM signal generator RF output level until the noise plus distortion increases to 3% THD or −30dB down. Then on Section 3 PCB, adjust L203 for maximum signal and minimum noise.

11. Set the FM signal generator to 106.1MHz or to a point of no interference either side of 106.1MHz with an RF output level of 1kμV (65dBf), 100% modulation (±75kHz) at 1kHz mono. Tune the MR 80 using the MAIN TUNING knob to 106.1MHz and switch PRESELECT (S601—Section 9) to the OUT position.

12. Reduce the FM signal generator RF output level until the noise plus distortion increases to 3% THD or −30dB down. Then on Section 3 PCB, adjust the slugs of C208, C215 and C217 for maximum signal and minimum noise.

13. Set the FM signal generator RF output level to 100μV (45.5dBf) and switch PRESELECT (S601—Section 9) to the IN position.

14. Reduce the FM signal generator RF output level until the noise plus distortion increases to 3% THD or −30dB down, and adjust C207 for maximum signal and minimum noise.

15. Switch PRESELECT (S601A—Section 9) to the OUT position. Using the MAIN TUNING knob, tune the MR 80 and the FM generator to 90.1MHz or to a point of no interference either side of 90.1MHz.

16. With the FM signal generator RF output level set for noise and distortion of 3% THD or −30dB down, adjust the top and bottom slugs of the MIXER TRANSFORMER (T201—Section 3) for maximum signal and minimum noise.

17. Repeat Steps 6 through 16 until no improvement is possible. The RF sensitivity with switch S601 (Section 9) in the OUT position should be 2.5μV (13.2dBf) or better, and distortion in mono at 1kμV (65 dBf) should be 0.2% or less. With switch S601 (Section 9) in the IN position, the RF sensitivity should be 5.0μV (19.1 dBf) or better.

E. **MULTIPLEX ALIGNMENT** (Sections 3 & 4)

1. Using the MAIN TUNING knob, tune the MR 80 and the FM signal generator to 90.1MHz, or to a point of no interference either side of 90.1MHz (±2MHz). Set the generator for 1kμV (65dBf), 100% modulation (±75kHz) at 1kHz mono.

2. Adjust FM OUTPUT LEVEL ADJUST (R905—Section 4) for 1V rms output at the fixed output jacks (on the back panel), channel balance should be within ±0.75dB.

3. Increase the FM signal generator RF output level to 10kμV (85.5dBf) and switch the generator to the CW mode (0% modulation).

4. Adjust the 19kHz ADJUST (R908—Section 4) for 19kHz (±20Hz) using either procedure a. or b. as follows.
   a. Using a frequency counter connected to Pin 34 on Section 7 PCB, adjust for 19kHz (±20Hz).
   b. Without a frequency counter: connect the multiplex generator 19kHz output to the horizontal input of the scope, connect a probe between the scope vertical input and Pin 34 on Section 7 PCB and switch the generator to stereo mode with 0% total modulation (0% pilot). Adjust the scope vertical and horizontal gain controls to obtain a square trace pattern. As you near the correct adjustment of R908, you will note that the trace is really not stationary but rotating on its axis. The correct adjustment of R908 is when the trace is stationary or very slowly rotating on its axis (within one rotation per second). Either side of the correct adjustment position of R908, the trace will rotate so fast that it will appear stationary.

5. Switch the FM signal generator to stereo, 1kHz right channel only, 100% total modulation (10% pilot). While monitoring the right channel output, establish a 0dB reference level on the distortion analyzer. Switch the generator to left channel only modulation and adjust the RIGHT SEPARATION ADJUST (R920—Section 4) for minimum right channel output (should be at least −50dB down).

6. Switch the FM signal generator to 1kHz left channel only, 100% total modulation (10% pilot). While monitoring the left channel output, establish a 0dB reference level on the distortion analyzer. Switch the generator to right channel only modulation and adjust the LEFT SEPARATION ADJUST (R921—Section 4) for minimum left channel output (should be at least −50dB down).

7. Repeat Steps 5 and 6 until no further improvement is possible.

8. Set the generator for 1kμV (65dBf) 100% modulation, ±75kHz at 1kHz mono. Adjust the FM OUTPUT LEVEL (R905—Section 4) for 1V rms output at the fixed output jacks.

9. Set the distortion analyzer to measure harmonic distortion. Switch the FM signal generator to stereo at 1kHz, 10kμV (85.5dBf), 100% total modulation (10% pilot), and measure THD in both left and right channels (should be 0.2% or less). If the measurement is higher than 0.2%, follow the procedure below.
   a. Adjust the top and bottom slugs of the MIXER TRANSFORMER (T201—Section 3) for minimum THD in stereo.
   b. Adjust the top and bottom slugs of the DETECTOR TRANSFORMER (T202—Section 3) for minimum THD in stereo.
   c. Switch the FM generator to mono, 100% total modulation, and measure the harmonic distortion (should be 0.2% or less) if not, repeat Steps a. and b. in mono.

d. If you cannot obtain 0.2% harmonic distortion in both mono and stereo, see note 3 in Section 3 notes and then start with alignment Step D.
e. Repeat Steps 5, 6 and 8 to obtain the best stereo separation.

10. Reduce the FM signal generator RF output level to 200μV (52.5dBf), in stereo at 1kHz, 100% modulation (10% pilot) and adjust the SIGNAL STRENGTH ADJUST (R262—Section 3) for 30dB of channel separation (R to L and L to R). This sets the stereo auto blend circuit.

F. **SUPER NARROW FILTER ALIGNMENT**
Sections 3 & 8)

1. Using the main tuning knob, tune the MR80 and the signal generator to 90.1MHz, or to a point of no interference either side of 90.1MHz. Set the generator for 2kμV (72dBf), 100% modulation (±75kHz) at 1kHz mono. Connect and adjust the scope for a centered multipath display and perform the following:
   a. Set the SELECTIVITY SWITCH (S1—Front Panel) to the SUPER NARROW position and adjust the FILTER OFFSET ADJUST (R331—Section 8) for maximum symmetry of the IF response curve either side of center.
   b. Adjust C241 (Section 3) for maximum IF gain and the best shape of the IF response curve.
   c. Return the SELECTIVITY SWITCH (S1—Front Panel) to the narrow position.

G. **MUTING AND FILTER ALIGNMENT** (Section 4)

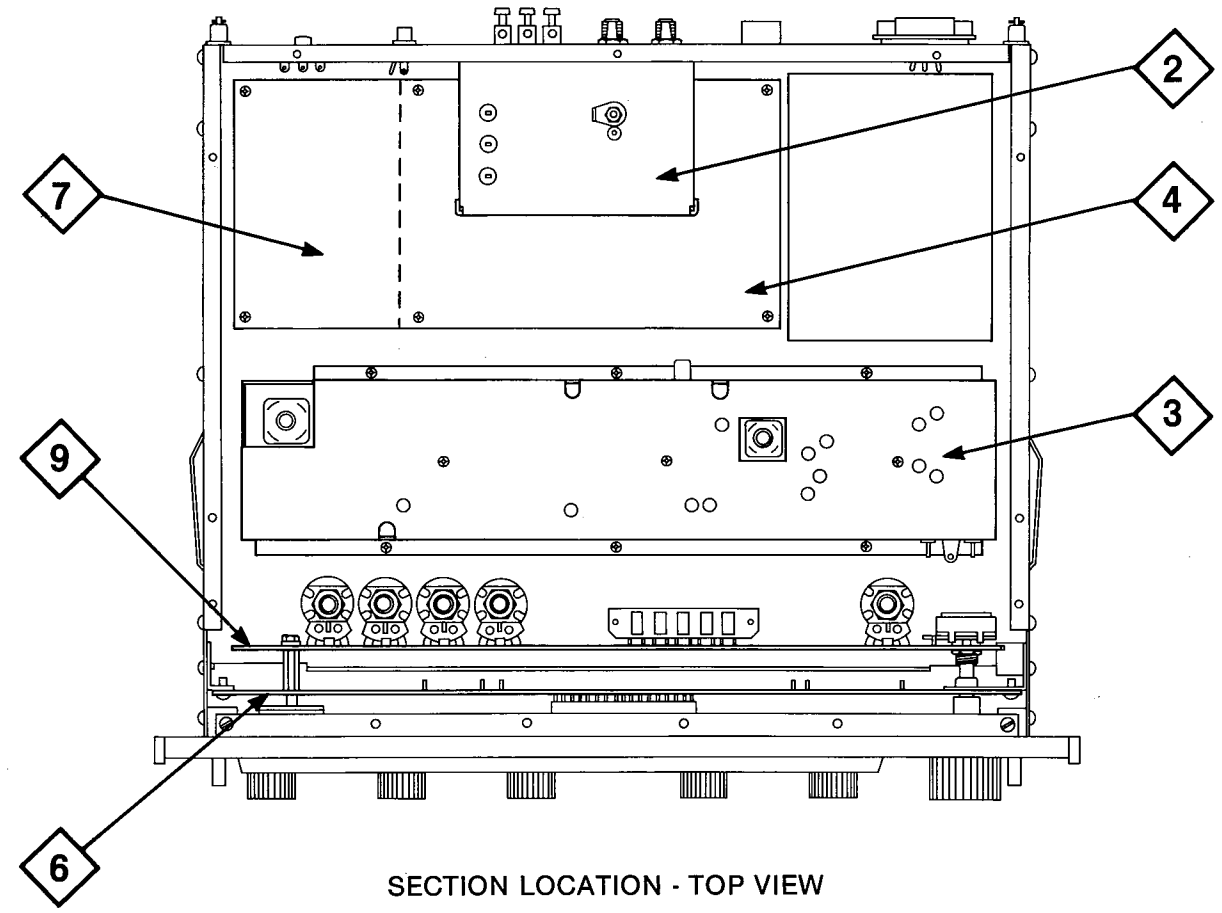
1. Using the MAIN TUNING knob, tune the MR 80 and the FM generator to 90.1MHz, or to a point of no interference either side of 90.1MHz. Set the generator for 2μV (11.2dBf), in mono at 1kHz, 100% modulation.

2. Turn the MUTING CONTROL (R6/S2—Front Panel) to minimum CCW position (just switched on) and adjust the MUTING ADJUST (R930—Section 4) so the tuner just mutes.

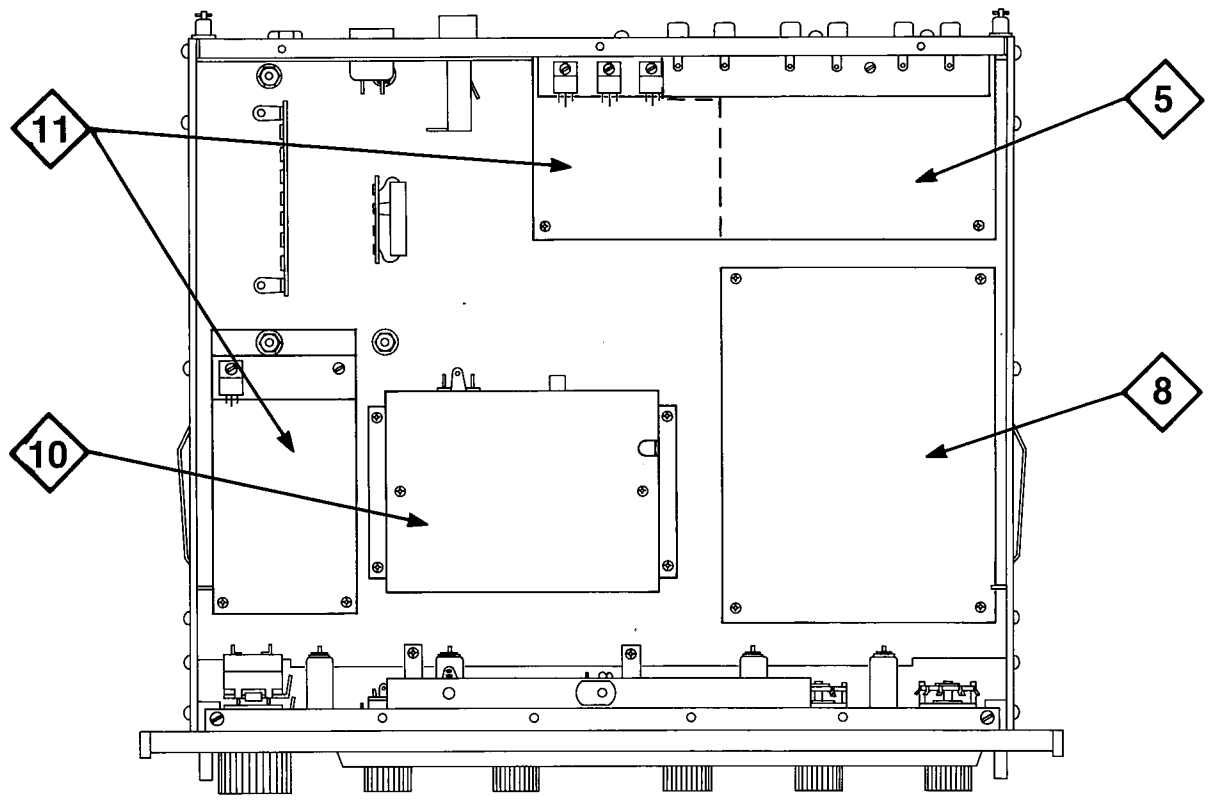
3. Switch the FM signal generator to 50μV (39.5dBf) in stereo at 1kHz, 100% total modulation (10% pilot) and switch the FILTER SWITCH (S4—Front Panel) to AUTO MODE, then adjust the FILTER LEVEL ADJUST (R940—Section 4) so that the filter light just comes on.

4. Switch the FM signal generator to mono mode and note that both the filter and stereo indicator lamps extinguish.

5. Switch the FM signal generator to stereo mode and increase RF signal level to 100μV (45.5dBf) and note that the filter lamp extinguishes.



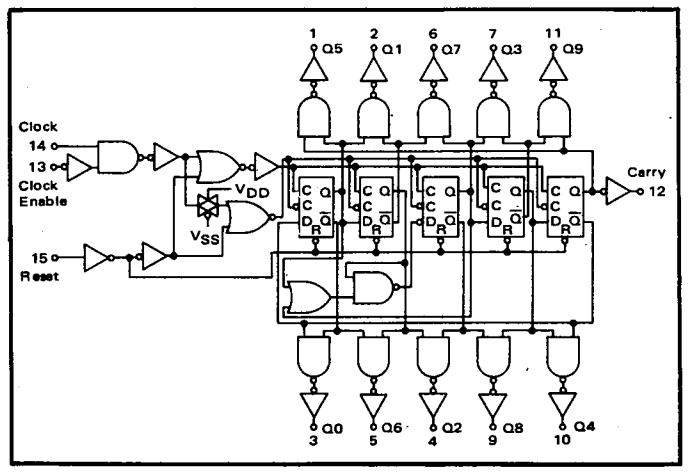
SECTION LOCATION - TOP VIEW



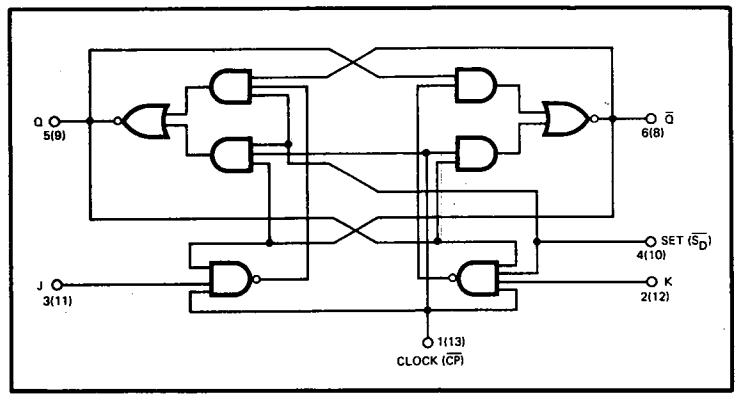
SECTION LOCATION - BOTTOM VIEW

Section 13

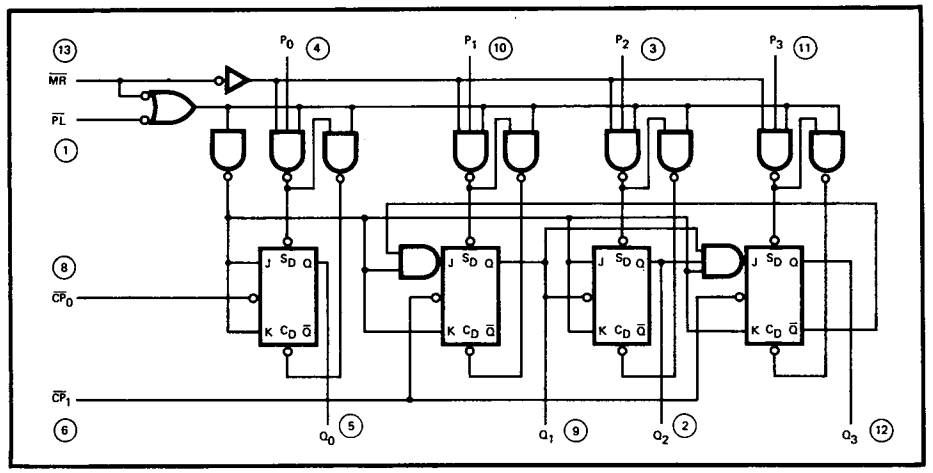
IC LOGIC DIAGRAMS and CIRCUIT OPERATION



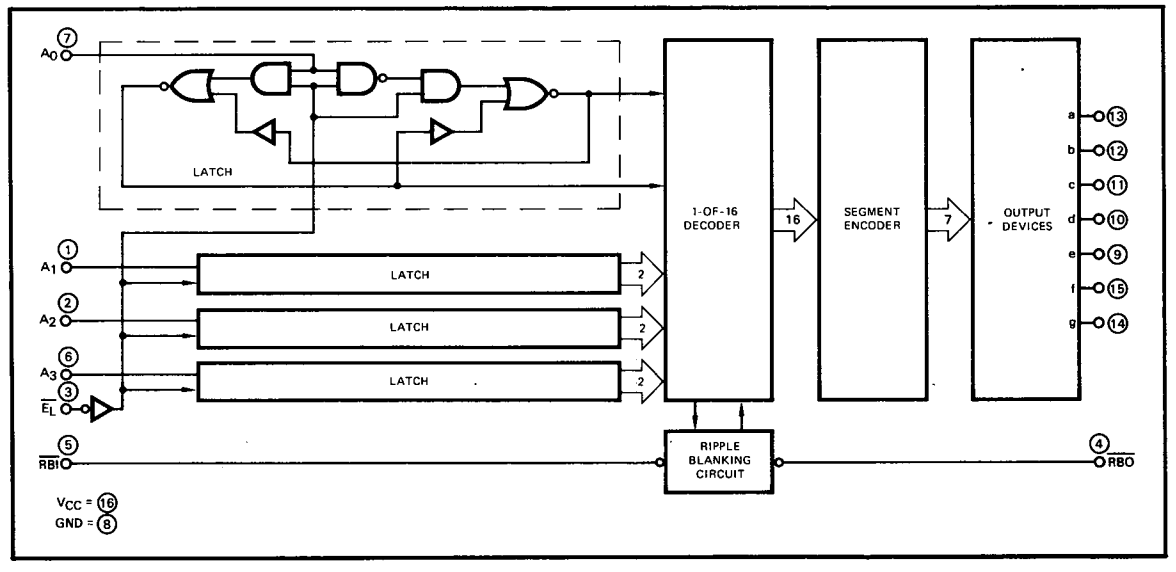
Logic Diagram 1



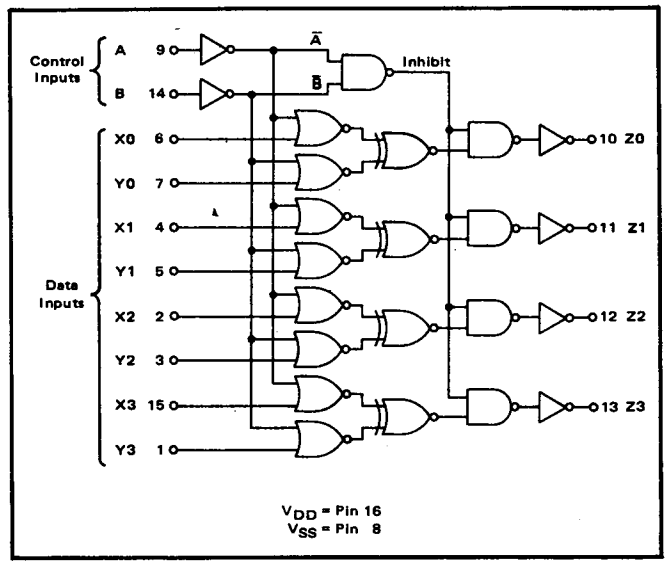
Logic Diagram 3



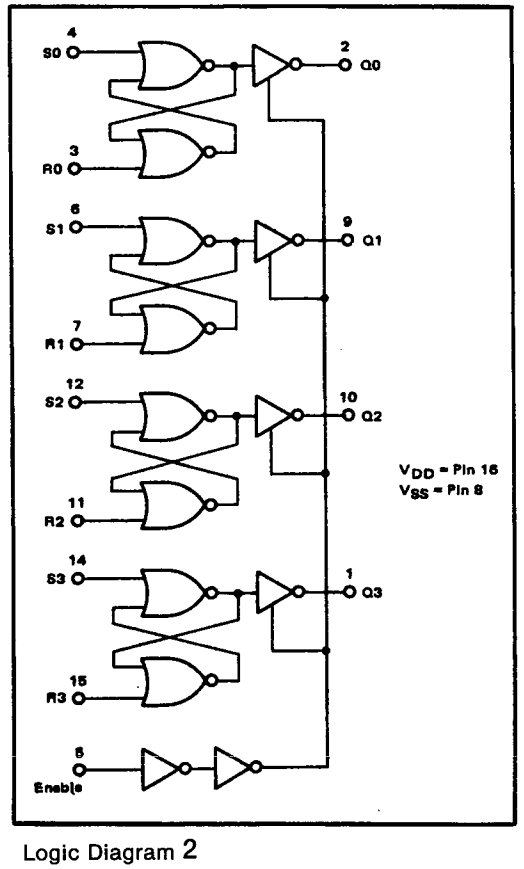
Logic Diagram 6



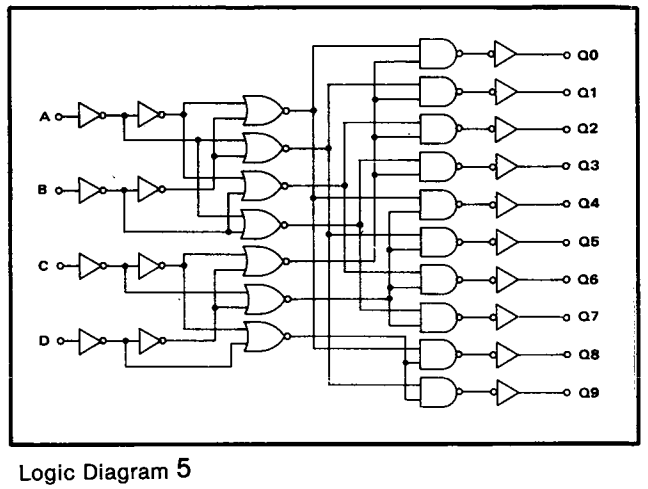
Logic Diagram 4



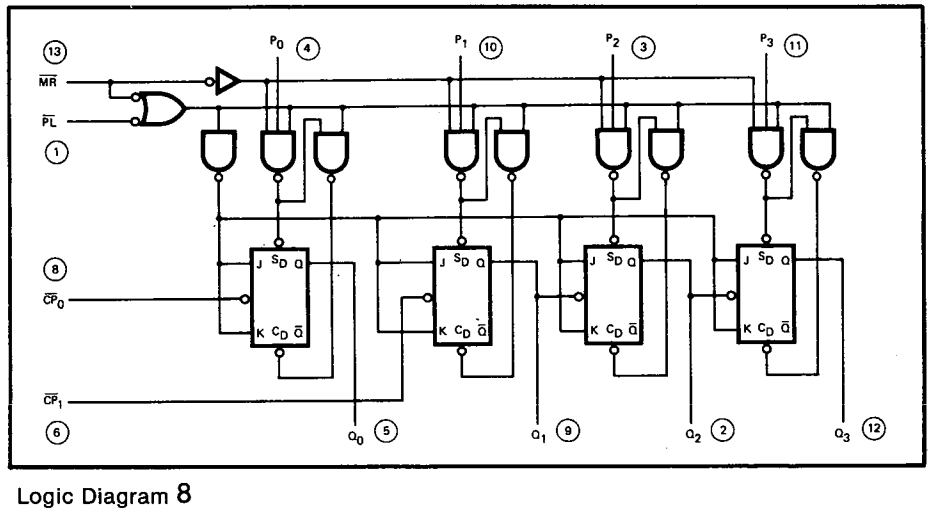
Logic Diagram 7



Logic Diagram 2

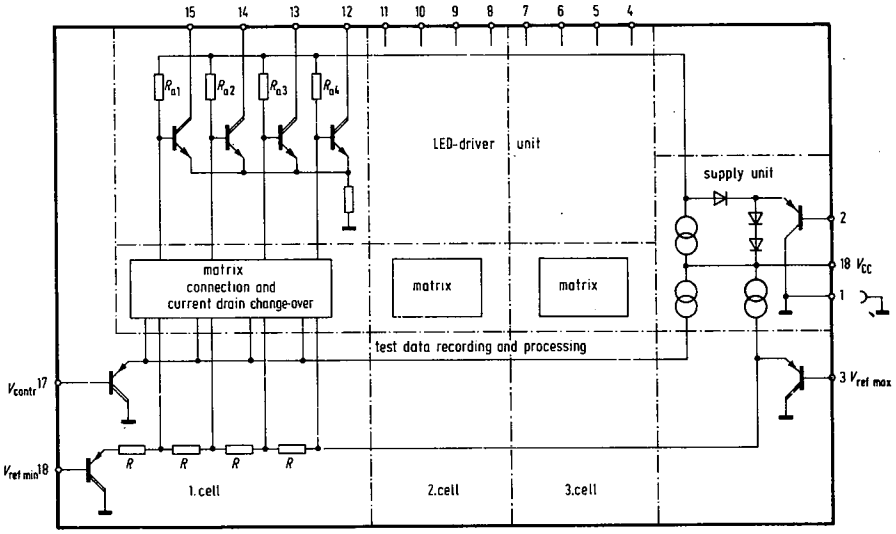


Logic Diagram 5

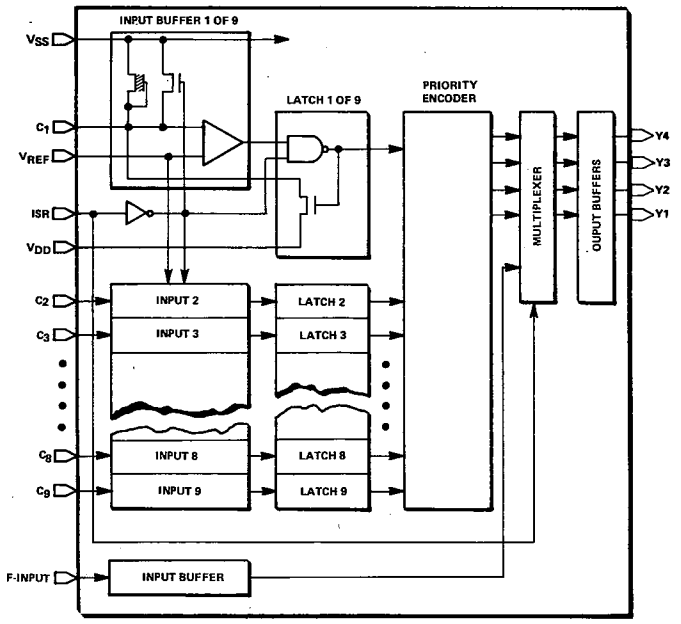


Logic Diagram 8

IC LOGIC DIAGRAMS and CIRCUIT OPERATION



Logic Diagram 9



Logic Diagram 10

Logic Truth Tables:

Gate Type

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

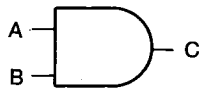
"Or"

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

"Nor"

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

"And"

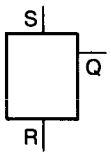


A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

"Nand"

S (set)	R (reset)	Q output)
0	0	No Change
0	1	0
1	0	1
1	1	1

"Flip-Flop"



CIRCUIT OPERATION

SECTION 1 and 11 - POWER SUPPLY

The transformer operated power supply provides critical voltages that are regulated and filtered by electronic networks to insure stable operation even with low line voltages. The power supply circuits are contained on the chassis and on two PC boards.

Line voltage is present at the unswitched receptacle at all times when the line cord is plugged in. Line bypass components consist of C1, C2 and R7. Main power On/Off is controlled by switch S6 (ganged with the volume control), and fuse F1 provides protection for the tuner. The main power transformer has two primary windings (allowing multi-voltage operation) and four secondary windings, three of which are center-tapped. The 5.6V AC winding, protected by fuse F2, supplies voltage to DS1 through DS4 and DS508 through DS510, all of which provide the necessary front panel illumination.

86.5V SUPPLY. The first center-tapped secondary winding (blue-yellow-blue) provides 32.5V AC (from center-tap to either end) which is rectified by diode bridge D704 and filtered by C708. The +86.5V is supplied to Q501 (the 19 kHz ϕ 1 amplifier-Section 6) and the constant current source circuit.

3mA CONSTANT CURRENT SOURCE. The constant current source circuit consists of Q701, D703, R701, R702, R703, R704, C709 and C710. The voltage drop across D703 is constant due to its zener action thereby forcing the voltage across R702 and the base emitter junction of Q701 to be constant. The voltage across R702 produces a constant current at the emitter of Q701, thus the collector current of Q701 is maintained at a constant 3mA. The constant current of 3mA is used by zener diode D601-Section 9, to maintain an extremely stable DC tuning voltage as is necessary for the varactor diode tuned front end.

+30V REGULATOR. The winding center-tap (first secondary winding) also supplies +39V (rectified by diode bridge D704) which is filtered by C714, for IC701 the +30V regulator. IC701 is a +15V three terminal IC regulator which provides a +30V regulated voltage because its common or reference input (Pin 2) is held at +15V above ground, thereby producing a regulated +30V output, filtered by C711.

±15V REGULATOR. The next secondary winding (red, yellow-red, red), center-tap grounded, is first rectified by diode bridge D702 and filtered by the combination of C703, C704 to provide ±22V. The +22V is supplied to the +15V regulator IC702, and further filtered by C712 to provide +15V for the tuner circuits and the +15V reference for IC701. In a similar fashion, the −22V is regulated by IC703 (the −15V regulator) and filtered by C713.

±10V SUPPLY. The last center-tapped secondary winding (green-gray-green) supplies 8V AC (from center-tap to either end) to the special circuits which drive the mode indication lamps (Section 6), is rectified by diode bridge D701, and is filtered by C701 and C702 to provide ±10V. The ±10V is also used by the monitor/headphone amplifier and by the LED tuning mode indicators. The −10V is used by the monitor/headphone amplifier.

+5V & −5.2V REGULATOR. The +10V is supplied to IC1 (+5V regulator) which provides +5V to the frequency counter circuits. The −10V is supplied to IC704 (−5.2V to regulator) which provides a regulated −5.2V to the circuits in Sections 8, 9 and 10.

SECTION 2 - ELECTRONIC ANTENNA SWITCH

The antenna switch assembly provides electronic switching of the incoming RF signal. The circuit basically functions as a single-pole, double-throw switch that allows the selection of two RF signal sources (such as FM antenna and cable FM), while providing greater than 75dB of isolation from the unused source.

ANTENNA SELECTION. When S601B is placed in the antenna position (−15V), D405 is reverse biased, D404 and D406 are forward biased, and the RF signal at Pin 5 is coupled to Pin 6. At the same time, D401 and D403 are both reverse biased, and D402 is forward biased to prevent the cable input RF signal from reaching Pin 6.

CABLE SELECTION. In a similar manner, when S601B is placed in the cable position (+15V); D401, D403 and D405 are forward biased; D402, D404 and D406 are reverse biased; therefore the cable input at Pin 4 is coupled to Pin 6, and the antenna input is prevented from reaching Pin 6. Resistors R401 through R404 provide current limiting, C401 through C405 are bypass capacitors, L401 and L402 act as DC bypass, along with L403 which is also the 300Ω to 75Ω impedance matching balun.

SECTION 3 - RF / IF ASSEMBLY

In this section, the incoming RF signal is tuned, amplified, converted to 10.7 MHz, further amplified and finally detected to provide the composite stereo output signal.

PRESELECTOR. The RF signal from Section 2 (antenna switch box) is connected to PCB pin 19, the RF input. The incoming RF signal has two possible paths to take upon entering section 3. If preselect switch S601A is placed in the OUT position, the RF signal is coupled by C203 directly to coil L204 through D205. This connection is made possible by diode electronic switching, and allows the RF signal to bypass the first tuned RF stage. With S601A in the OUT position, - 15V DC is coupled through C201 and L201 (line filters) to PCB pin 17, where D202 is reversed biased, thereby preventing the RF signal from reaching the first tuned RF stage. At the same time, D201 is forward biased to short out the first tuned RF stage so its loss is not coupled into the circuit. The first tuned RF state consists of L203, D203, D204, C207 and is coupled by C287 to the second RF tuned circuit. At the same time, D205 is forward biased on, and the RF signal is coupled to the second RF tuned circuit. D205 is tapped onto L204 to yield optimum signal to noise and together with D207, D206 and C208, form the second tuned RF stage. If preselect switch S601A is placed in the IN position, + 15V is made available at PCB pin 17. This + 15V reverse biases D201 and D205 off, and forward biases D202 on, and the RF signal is coupled by C204 to the first tune RF stage. Diode D202 is tapped on L203 to yield optimum RF selectivity. When the first and second RF tuned circuits are in operation, (S601A in the IN position) a very high circuit Q is formed which provides a sharp bandpass.

RF AMPLIFIER. The RF signal from L204 is connected to the gate input of Q201. Q201 is a rugged J-FET transistor and forms an impedance converter. Q202 is a high power RF amplifier and together with Q201 form a cascode amplifier. This circuit allows high gain, low noise and high output levels without the need for neutralization. The output of the cascode RF power amplifier is coupled to the third tuned RF stage (L206, C215, C214, D208 and D209), and in turn to the fourth tuned RF stage (D210, D211, C217 and L207). The third and fourth parallel tuned RF stages are used to provide selectivity and the proper load impedance for the cascode RF power amplifier thereby improving the image rejection and overload performance of the tuner.

BALANCED MIXER. C219 couples the RF signal to the low-loss toroidal phase splitting Coil L208. Coil L208 feeds the matched dual J-FET balanced mixer circuit consisting of Q203 and Q208. Mixer transformer T201 is balanced and double tuned, and is used as the drain load of the balanced J-FET mixer circuit. Transistor Q204 serves a dual function; a buffer amplifier for the oscillator and a constant current source for the dual J-FET mixer circuit. Variable resistor R224 (Mixer bias adjust) permits the optimum amount of bias for Q203 and Q208 to achieve the lowest IM distortion and noise level.

OSCILLATOR. Transistor Q205 together with L211, D212, D213, C227, L212 and C231 form a parallel tuned oscillator circuit that is always tuned 10.7MHz higher than the frequency of the desired FM station. Resistors R226 and R227 form an impedance match for driving the coaxial cable connecting the front-end oscillator to the frequency counter.

VARIABLE SELECTIVITY. Front panel selectivity switch (S1) allows two degrees of IF selectivity-narrow and super narrow. If switch S1 is placed in the narrow position, − 15V goes to the cathode junction of D215 and D216 and forward biases them on. This connects the IF signal from T201 pin 3 to the input gate of J-FET Q207. PCB Pin 9 is at ground potential, when switch S1 is in the narrow position, allowing Q207 to pass the IF signal to the first IF amplifier IC201. If switch (S1) is placed in the super narrow position, + 15V is at the anode connections of D214, D217, and D218 (they were biased off in the narrow position of S1), and they are now biased on. Capacitor C239 couples the IF signal through D214 to FN201, the 4 pole 4 zero Quartz filter, and on to the gate input of J-FET Q206. PCB Pin 10 is now at ground potential and Q206 passes the IF signal to the IF amplifier IC201. D217 and D218 in the super narrow position are biased on to shunt any remain signal that may be coupled by stray capacitance through Q207.

IF AMPLIFICATION. The IF signal coming from the super narrow selectivity circuit is coupled by capacitor C249 to the first IF amplifier stage. IC201 (first IF amplifier) is operating at a higher supply voltage level to increase the overload capability of the tuner. IC's 201, 202, 203 and 204 are high gain differential amplifiers and together with FN202, FN203, FN204 and FN205 (Piezoelectric 10.7MHz filters) all together comprise the narrow selectivity circuit and provide the necessary amplification.

LIMITING & DETECTION. IC205 (FM gain block) starts the limiting process and its output is coupled to IC206 through FN206 and C277. IC206 completes the limiting process and also drives the discriminator transformer T202. The IF signal is detected by diodes D229 and D230 to provide the composite signal output.

SIGNAL STRENGTH OUTPUT. At the secondary outputs of IC201 through IC205 are full wave rectifier diodes D219 through D228. All the rectified outputs are combined and fed to IC207, the signal strength summing amplifier. The output of IC207 drives the auto stereo blend, muting and auto filter circuits in Section 4.

TUNING VOLTAGE. The tuning voltage from Section 9 enters at Pin 18A and goes through C235 and L214 to R230 and C238 which filter out noise that

may be present on the tuning voltage. Resistor R231 provides temperature compensation of the tuning voltage for the circuits in this Section. The value of R231 sets the current which flow in diodes D604 to D608 in Section 9. This current level and the current/temperature characteristics of D604 to D608 compensates the tuning voltage.

SECTION 4 - MULTIPLEX, FM MUTING & NOISE FILTER

The composite signal coming from the detector is frequency compensated by R903, C901 and is fed to IC901 which acts as a buffer amp to prevent detector loading. The amplified composite signal is fed to Pin 29 of Section 8 (where it is used to process the lock control) to the muting circuits, to the horizontal (TP-2) output jack for multipath display and lastly to IC902 (the phase locked loop stereo decoder.) C906 couples the composite signal from IC901 and IC902.

MPX VCO. The internal voltage controlled oscillator (VCO) free running frequency of 228 kHz is determined by R907, R908, R909 and C905 and is adjusted by R908. The 228 kHz is used internally in IC902 and is also fed to Section 7 to provide signals which operate the input touch control circuitry.

AUTO BLEND. Pin 11 of IC902 is the control input for the auto blend circuit so that channel separation varies as the RF signal level varies. If the DC voltage at the cathode of D901 falls below +4.2V, D901 becomes forward biased and Pin 11 of IC902 is pulled negative thereby reducing channel separation. C950 is used to stabilize the blend circuit under conditions of rapidly changing RF to prevent the channel separation from also varying rapidly.

C907, C908 and R918 determine the frequency capture range of the PLL circuit; R983, R982 and D907 provide input coupling and isolation for the stereo/mono switch circuitry of IC902, so when you tune off of the station, IC902 is switched to mono and prevents false triggering on interstation noise. "Nor" gate IC903A acts as an inverting switch for the FM stereo indicator lamp and auto filter "Nand" gate IC904B. C913, R924, C915, R925 together with components on Section 9 PCB determine the necessary de-emphasis curve for flat frequency response on both channels.

AUTO FILTER. The auto filter voltage comparator circuit consists of IC907 and associated components. R940 determines the threshold point of IC907 by varying the DC level at Pin 3 while Pin 2 is fed voltage which is directly proportional to the RF signal strength (coming from IC207 on Section 3). When the signal strength voltage is above the setting of R940, the output of IC907 is low, and the output is high if the signal strength is below the setting of R940. IC904B is a "Nand" gate which changes its state only when the RF signal strength is below 50μV (determined by IC907) and in stereo. If the station received is in stereo with RF signal strength of 50μV or below (switch S4 is in the AUTO FILTER or ON mode), Pins 2 and 7 of IC906 (quad J-FET electronic switch) go low thereby switching in the twin T notch filter (C924, C925, R939, R947, R945, R946 and C945) that blends the high and low frequencies leaving separation unaffected at mid-frequencies. At the same time, inverting "Nor" gate IC903D switches on the auto filter lamp.

MUTING DRIVE. The tuner mutes when tuned off station and/or tuned to a weak signal. IC905 is a deviation detector whose output voltage switches between −14V when on station to +14V off station and/or when noise is present from the noise amplifier. C909, C918, L901 and C917 together form a bandpass filter centered at 138kHz which feeds ultrasonic noise components to the amplifier Q901. The amount of the noise that is coupled to the base of Q901 (the noise amp) is determined by the setting of R930 (muting adjust control). R930 is also part of the Q901 bias voltage divider including R931 and R984. In order to prevent the muting circuit from inadvertently muting on pulse noise, the gain of Q901 is decreased when tuned to a station. R929 increases the gain of Q901 when tuned off station due to IC905 whose output goes to +14V thereby increasing the amount of bias on the base of Q901. If you are tuned on station, the output of IC905 goes to −14V, the DC bias goes down and the gain of the noise amp Q901 is reduced. C921 couples the output of the noise amp to IC905 which also causes the output to change state in the presence of noise, and IC905 feeds IC904A through R928. D904 acts as a negative voltage clamp to protect the inputs of "Nand" gate IC904A which is used as an inverter.

MUTING THRESHOLD. IC908 is a signal strength muting comparitor amp to compare the incoming signal strength to the front panel muting control position (R6). R950 and C946 together form a time constant to give the circuit hysteresis. The output of IC908, together with the output of "Nand" gate IC904A, are fed into "Nand" gate IC904C which changes state when there is noise (and/or mistuning), or if the RF signal strength is below the threshold setting of R6.

"Nor" gate IC903C switches the lock lamp on only when the tuner is unmuted and two seconds after tuning has stopped. "Nand" gate IC904D is used as an inverter which controls the scan stop circuit (on Section 8), and drives "Nor" gate IC903B whose output only goes to logic level "1" (muted condition) with the muting switch in the ON position together

when a muting condition from IC904D occurs. D906, R959, R958, C932 and R957 form an RC time constant with turn-off decay to provide a quick mute-on and a delayed mute-off condition. With a mute control signal present at Pins 10 and 15 of IC906, both electronic switches open and stop the signal flow.

FILTERING. IC909 and IC910 provide the necessary drive and correct source impedance for FN901 (19 and 38 kHz filter). IC911 and IC912 together with R and C components provide audio bandpass filtering to eliminate unwanted noise and transients below 20 Hz and above 20 kHz. C933, R970, C934 and R971 form a high pass filter. R975, C937, R976 and C938 form a low pass filter network for the left channel, with the corresponding components in the right channel performing identical functions.

SECTION 5 - HEADPHONE AMPLIFIER & TURN-ON DELAY

The turn-on delay circuit provides transient free turn-on and turn-off characteristics. At the moment when power is first applied, Q808 is non-conducting and therefore no current will flow through the diode portions of LDR801, LDR802 and a very high resistance is exhibited by the resistor elements since these elements are in series with the audio output. Resistors R811, R812 form a voltage divider to bias Q808 on approximately two seconds after the first turn-on due to the long time constant of R811 and C804. When power is turned off, R812 quickly discharges C804, then Q808 is switched off and mutes the output before the main power supply has a chance to discharge. Resistor R804 limits current flowing through both LDR's and Q808.

HEADPHONE AMPLIFIER. The headphone amplifier circuits for both channels are identical so that only the left channel will be described. C801 and R801 couple the input signal coming from the volume control R8B to the differential amplifier consisting of Q802 and Q801. The current source R802 provides high input impedance with low noise. The base of Q801 is grounded to maintain the output stage at zero volts DC offset; the base of Q802 is supplied with both the input signal as well as the negative feedback path formed from R805 and C802. Q806 and Q807 function as the current mirror circuit for the differential amplifier and drive Q805 (Class A voltage amp). R803 is the load resistor for Q805. D801 is used in the class AB DC biasing circuit for the complimentary output transistors Q803 and Q804. Resistors R806 and R807 limit the current flowing through the output transistors. A voltage divider is formed by R809 and R810 to provide 2.5V AC at 600 ohms at the left variable output jack, and R808 limits the current to the headphones. C803 controls the high frequency stability of the overall amplifier.

FILTERING. Power supply filtering and decoupling for the turn-on delay and headphone amplifier is performed by C808, C810 and R822 for the + 10V supply. The same is true for C809, C811, R823 for the – 10V supply.

SECTION 6 - TOUCH CONTROL DISPLAY FUNCTIONS

Transistor Q501 and its associated components amplify the 19kHz ϕ1 signal coming from Section 7 PCB. The 75Vp-p of the 19 kHz ϕ1 signal, from the collector of Q501, is coupled by C517 and C516 to pins 12 and 13 of IC501 (two unused touch sensor inputs), and to capacitors C502 through C508. Capacitors C509 through C515, and current limiting resistors R504 through R508, R535 and R536, couple the 19kHz ϕ1 signal to the active touch sensor inputs of IC501. Since IC501 is an NMOS device it is vulnerable to static discharge damage when the touch buttons are touched. Neon lamps DS501 through DS507 provide protection for the touch sensor inputs, Pins 5, 6, 7, 8, 9 and 10.

TOUCH ENCODER. IC501 contains input buffers, latches, BCD priority encoder, multiplexer and output buffers. When a front panel touch button is touched, the stray capacity of the human body shunts some of the 19kHz ϕ1 signal to ground. The input buffers are normally at a high level, and when the touch sensor is touched, the level goes low which is detected by the input buffers. A 19kHz ϕ2 signal from Section 7 PCB is directly coupled into pin 15 of IC501. This 19kHz ϕ2 signal is used to transfer the outputs of the input buffers into the latches. The latches are used as temporary storage to prevent false triggering due to static and voltage transients. From the latches, the signal is coupled to the priority BCD encoder. The priority encoder functions such that if the Preset 2 touch button is touched continuously and Preset 1 is also touched, the tuner will go to Preset 1; if 2 and 3 are touched, at the same time, the tuner will go to Preset 2. The priority of the input touch sensors from the highest to the lowest priority is as follows; main tuning knob, Preset 1, 2, 3, 4, scan up and scan down. Touch sensitivity adjustment R509 allows the input-compare levels to be adjusted for the capacitive inputs. The 3 bit binary coded decimal output of IC501 is coupled to IC502 pins 10, 13 and 12.

TOUCH DECODER. IC502 is a 3 bit BCD input to an octal decoded line output decoder circuit. Resistors R510 through R513 are the pulldown resistors for the four outputs of IC501. IC502 reconverts the BCD in-

put word back into a one of seven line code, providing an output indicating the front panel touch button sensor that is touched. The 76kHz reference signal from Section 7 is directly coupled into pin 11 of IC502. This 76kHz reference signal is the phase reference that inhibits the decoder during the leading and trailing edges. This is done to prevent false decoding of the BCD signal due to noise glitches and/or partial finger contact with the front panel touch buttons. Capacitors C518 through C522 remove any spikes that may be present on the decoder line outputs of IC502. The seven line outputs connect to Section 7.

DIGIT DRIVER. DS518, DS519, DS520 and DS521 are seven segment common cathode LED digital readouts. The tens, units and fraction readouts are driven directly by IC503, IC504, IC505 respectively. IC503 through IC505 are (BCD input to LED driver output) devices that contain input latches, a 1 of 16 decoder, a seven segment encoder and constant current source LED drivers. Pin 3 of the IC's is the latch enable input and receives the display enable gating pulse from Section 10. When the gating pulse goes negative, 12 times a second, the input latches couple the BCD code at input pins 1, 2, 6 and 7 to the decoder so that the LED display can be updated. The display blanking control signal at pin 32 is coupled through R537 to Q511. Q511 is normally reversed biased off and pin 4 of IC503, IC504 and IC505 is kept high. When the blanking input (pin 32) goes high, Q511 is forward biased on blanking the display by pulling low pin 4 of IC503, IC504 and IC505.

The hundreds LED display is switched off when the frequency of the station is below 100.0MHz and shows the digit 1 when tuned to a station at 100.0 MHz or above. If the tuner is tuned below 100.0MHz, the center segment of DS519 is on as the digit would be either a digit 8 or 9. Pin 14 of IC503 would be high and thereby reverse biasing Q503 off thereby blanking the hundreds display. When the tuner is tuned to 100.0 MHz or higher, the center segment of DS519 is off, (the digit would be a zero) and pin 14 of IC503 goes low. This forward biases Q503 on which in turn switches on Q502 and grounds pin 8 of DS518, (the common cathode connection) thereby illuminating the digit 1. The output of Q503 is also sent to sections 8 and 10 through PCB pin 39 to speed up the scanning rate when above 100.0MHz. R514 and R515 limit the current to the LED segment of DS518, and C523 bypasses the 5 volt supply. The display blanking input at pin 32 is also connected to the base of Q503 by the voltage divider consisting of R518 and R519.

TUNING MODE INDICATORS. Transistors Q504 through Q510 are used as electronic switches to turn on the appropriate front panel LED lamps to indicate what tuning method is in control. Resistors R523, R525, R527, R529, R531 and R533 limit the current flowing through their respective indicating LEDs.

SIGNAL STRENGTH. DS517 is a 12 segment LED bar display driven by IC506. The signal strength DC voltage input at pin 45 (section 3) is connected through voltage divider R538 and R539 to the control input pin 17 of IC506. Signal strength adjust R643 allows the operator of the tuner to adjust the sensitivity of the signal strength display by varying the DC voltage at pin 3 of IC506. Transistor Q512 is used as an electronic switch to blank the signal strength display by grounding pin 2 of IC506.

MODE INDICATION. The front panel mode incandescent indicator lamps, Stereo, Lock and Filter, are driven by a special circuit to greatly extend the operating life of the lamps. The lamps are driven by AC voltage instead of the more commonly used DC voltage which cause lamp failure due to the DC notching effect.

All three lamp circuits are identical except for the resistor values of R544, R551 and R545 so that only the stereo mode circuit will be described. When the control voltage at pin 3 goes high, the voltage of Zener diode D501 is exceeded and transistor Q513 is biased on due to the voltage drop across R546. Current is allowed to flow during both positive and negative halves of the 8V AC line at pin 5 thereby operating lamp DS522 on AC current. Resistor R544 limits the current flowing through DS522 to also extend the useful life of the lamp. When the control voltage at pin 3 goes low, Zener diode DS501 prevents current from flowing through R546 thereby keeping Q513 reversed biased off.

DS508, DS509, DS510 provide upper left side front panel illumination.

SECTION 7 · PRESET SCAN & TOUCH CLOCK

Preset station selection and remote control is provided by the circuitry contained in this section. IC1003 is a quad two channel data selector and controls both front panel and remote control selection of the four presets.

REMOTE PRESET. If one of the four station preset touch buttons on the front panel is touched, a pulse is generated by Section 6 circuitry, placed on the appropriate input line to Section 7 (Pins 46, 45, 44 or 43), and is coupled directly through IC1003 (which functions the same as a 4 pole double-throw switch) to output lines (Pins 49, 50, 51 or 52). When switch S3 is placed in the PRESET mode and the REMOTE CONTROL (momentary switching) pushbutton is

depressed, several things happen. First a negative pulse is generated which is inverted by "Nor" gate IC1001A to toggle the flip-flop circuit (consisting of IC1001B and C), and places a logic level of "1" on the emitter of Q1001 which in turn switches Q1002 on. This connects the output of IC1004 (the decade counter) to the other four input lines X0 through X3 of IC1003. At the same time, the positive pulse from "Nor" gate IC1001A is sent to Pin 14 of IC1004 (the clock input), and forces IC1004 to generate a pulse on the next data output line (Q0, Q1, Q2, Q3).

REMOTE SCAN. If S3 is in the SCAN ALL position, a negative pulse is likewise generated toggling the flip-flop circuit (IC1001B and C) to provide a logic level of "0" for Pin 13 of "Nor" gate IC1001D, together with a logic "0" on Pin 12, forcing a positive pulse at the output of IC1001D. This positive pulse is then sent to Section 8 to the scan start circuitry. With S3 in the SCAN ALL position, logic "1" is present at Pin 9 of "Or" gate IC1002A causing a logic "1" to Pin 1 of "Nor" gate IC1001B, and a logic "0" at the emitter of Q1001 which is reverse biased off. This resets IC1003 to connect the front panel touch input lines to the output lines of Section 7. Diodes D1001 through D1008 form an "Or" gate and function in a similar manner as the remote SCAN ALL, to return control to the front panel touch preset buttons.

POWER-ON CLEAR. A power-on clear pulse from Section 8 circuitry resets IC1004 through "Or" gate IC1002B to reset the counter so that the first time the remote button is pushed preset PS1 is the first preset selected. Diodes D1009 through D1014 couple the pulses of the unused counter outputs (Q4 through Q9) to reset IC1004 from Q0 to Q3 so that the tuner goes from preset PS4 back to preset PS1. The reason you do not see preset PS4 as on is because on power turn-on, the main tuning knob is always activated first. The power-on clear pulse also toggles the flip-flop circuit (IC1001B and C) so that IC1003 always "reads" the input lines from Section 6 circuits (front panel touch buttons). R1003, C1001 and R1004, C1002 form two debounce networks to prevent false triggering of the circuits.

TOUCH CLOCK. The circuit involving IC1005, IC1006 and IC1007 divide the 228kHz clock signal obtained from the MPX IC, IC902 Pin 15. "Nor" gates IC1005A and B are biased on as an amplifier and the 228kHz signal is coupled to Pin 8 and 9 via C1004. IC1006A and B is connected as a shift registor (dividing by 3) to provide a 76kHz reference signal out of Pin 36, and is further divided by 4 in shift registor IC1007A and B. The two 19kHz signals are then gated by IC1005C and D to provide non overlapping two phase signals for the touch circuits on Section 6.

SECTION 8 - CONTROL LOGIC,TUNING VOLTAGE & TUNING LOCK

This section performs the following major functions: Control Logic, Up/Down Scan Tuning Voltage, Tuning Lock, Blanking, and Power On Clear.

POWER ON CLEAR. The power on clear circuit is used to provide the various timed sequences and delays for proper noise free operation of the tuner. IC309A is a monostable multivibrator with an output that goes high during the first 4 seconds the tuner is turned on. When the main power is turned ON, pin 2 of IC309A is at logic "0" and pin 6 goes to logic "1". The logic "1" at pin 6 of IC309A (Power On Clear) performs the following:

1. The lock lamp and tuning lock circuit are turned OFF. D308 is forward-biased ON, and a logic "1" is at pin 13 of "Or" gate IC306A.

2. The scan run/stop flip-flop is reset. D308 is forward-biased ON, a logic "1" is at pins 9 and 10 of "Or" gate IC305B, and a logic "1" is at pin 7 of IC307D.

3. The scan on/off flip-flop is reset. D308 is forward-biased ON, a logic "1" is at pin 13 of "Or" gate IC312C, and a logic "1" is at pin 11 of IC307C.

4. The main tuning knob flip-flop is set. D308 is forward-biased ON, a logic "1" is at pin 14 of IC307B, and pin 1 (the Q output) of IC307B goes to logic "1" and activates the MAIN TUNING knob.

5. Presets 1 thru 4 are reset. D308 is forward-biased ON, and pin 2 of "Or" gate IC304D is high causing a logic "1" at pin 3. This in turn places a logic "1" at each of the presets 1 thru 4 "Or" gates: pin 5 of IC302B, pin 9 of IC302A, pin 5 of IC303A, and pin 9 of IC303B.

6. The remote control preset decade counter is reset in Section 7. IC309A pin 6 goes to logic "1" and is connected by PCB pin 35 to Section 7.

7. The audio mutes in Section 4. D309 is forward-biased ON, and a logic "1" is connected to Section 4 by PCB pin 30.

Resistor R304 and capacitor C302 form an RC time constant of approximately 4 seconds. Four seconds after turn-on, pin 2 of IC309A goes to a logic "1" and resets the output of IC309A (pin 6) to a logic "0".

Diode D307 quickly discharges capacitor C302 when the main power is turned OFF. R303 and C301 also form an RC time constant and are used to keep pin 4

of IC309A at a logic "1" during power line transient spikes. D306 discharges capacitor C301 upon power turn-off.

BLANKING CIRCUIT. The blanking circuit consists of IC310B (debounce time one-shot) and IC310A (blanking time one-shot). The output of the blanking circuit (pin 10 of IC310A) supplies a logic "1" when activated and performs the following:

1. The digital frequency display and the signal strength indicator are blanked. PCB pin 31 connects to pin 32 of Section 6 thru Section 10.

2. The audio signal is muted. Diode D313 is forward-biased ON, and the logic "1" at pin 30 is used to activate IC906 in Section 4.

"Or" gate IC306B provides a logic "1" at the output (pin 9) when the MAIN TUNING knob, PRESETS 1 thru 4, SCAN UP/DOWN or REMOTE SCAN ALL functions are activated. IC310B is set up to provide the necessary debounce time to prevent false triggering of the blanking monostable of IC310A. When main power is turned ON, pin 2 of IC310B is low, and the output (pin 6) is at a logic "1". This activates the blanking time one-shot, which in turn blanks out the displays and mutes the audio for approximately 2 seconds until the tuner stabilizes. A logic "1" at pin 4 pulls pin 2 of IC310B low (logic "0"), and this discharges capacitor C306. With pin 2 at logic "0", the output at pin 6 of IC310B goes high (logic "1"). R316 and C306 form an RC time constant, and when C306 charges up again, this forces pin 2 high, and pin 6 of IC310B goes to a logic "0". IC310A functions in an identical manner to IC310B. Due to the longer time constant of R307 and C304, resistor R333 ensures that C304 is discharged when pin 14 of IC310A goes low.

MAIN TUNING KNOB. Upon touching the MAIN TUNING knob, a positive-going pulse is generated in Section 6, coupled thru Section 7, and arrives at PCB pin 42. Diode D305 is forward-biased, and a positive pulse appears at pin 14 of IC307B. When pin 14 of IC307B goes high (logic "1"), the following things happen:

1. Presets 1 thru 4 flip-flops are reset. Pin 2 of "Or" gate IC304D is high, causing a logic "1" at pin 3, and this in turn places a logic "1" at the input of each "Or" gate for presets 1 thru 4.

2. The scan on/off flip-flop IC307C is reset thru "Or" gate IC312C.

3. The scan run/stop flip-flop IC307D is reset thru "Or" gate IC305B.

4. The lock lamp delay circuit is toggled which consists of IC308B, C, D, and A.

5. The lock circuit is turned off. Pin 10 of IC306A goes to a logic "1" which in turn forward-biases D316 ON, and pin 3 of IC313 is forced high.

Flip-flop IC307B is set to a logic "1" at the Q output terminal. This logic "1" (at pin 1 of IC307B) performs the following:

1. The manual lock circuit is activated. Pin 8 of "And" gate IC311A is at a logic "1" and if the LOCK switch is OFF, a logic "1" is also at pin 9 of IC311A. Pin 10 of IC311A is then high and D311 is forward-biased ON, thereby placing a logic "1" at PCB pin 28. This turns off the LOCK lamp and keeps it off. Diode D315 is also biased ON and pin 3 of IC313 is forced high.

2. The main tuning potentiometer is activated. The logic "1" at pin 1 of IC307B is directly coupled to PCB pin 14. PCB pin 14 is connected to Section 9 PCB pin 8 where transistors Q608 and Q602 are switched ON, and the main tuning potentiometer R610 is activated.

The output of "Or" gate IC312B (pin 10) is connected to pin 15 of IC307B (the knob flip-flop). Pin 9 of IC312B goes to a logic "1" when any of the PRESETS are activated. Pin 8 of IC312B goes to a logic "1" when SCAN UP/DOWN or REMOTE SCAN ALL are activated.

When either pins 8 or pin 9 of "Or" gate IC312B goes high, the output (pin 10) also goes high. The logic "1" at pin 15 of IC307B resets the knob flip-flop's Q output (pin 1) to a logic "0".

The output of "And" gate IC311B goes high when going from PRESETS or SCAN to MAIN TUNING knob. This generates a single pulse to trip the debounce time one-shot IC310B thru IC306B, which in turn momentarily blanks and mutes the tuner.

PRESETS 1 THRU 4. Upon touching any one of the PRESET touch buttons, or activation of the remote preset circuit (Section 7), a positive-going signal will be at one of the Section 8 PCB pins 40, 39, 38, or 41. The circuits of presets 1 thru 4 function identically so that only preset 1 circuitry will be described.

A positive-going signal from Section 7 enters at PCB pin 41 and goes in two directions. When pin 4 of "Or" gate IC305A goes high, the output at pin 1 goes to a logic "1" and performs the following:

1. The lock circuit and lock lamp turns off. IC306A pin 10 goes to a logic "1".

2. The main tuning knob flip-flop IC307B resets.

IC312B pin 10 goes to a logic "1".

3. The scan on/off flip-flop IC307C resets. IC312C pin 11 goes to a logic "1".

4. The scan run/stop flip-flop IC307D resets. IC305B pin 13 goes to a logic "1".

5. The blanking circuit is activated. The output of "Or" gate IC306B goes to a logic "1" and toggles IC310B, the debounce time one-shot.

The second direction the positive-going pulse at PCB pin 41 goes to is as follows:

1. Preset 4 flip-flop IC301D resets. A logic "1" at pin 12 of "Or" gate IC303B causes a logic "1" at IC301D pin 7.

2. Preset 2 flip-flop IC301C resets. A logic "1" at pin 2 of "Or" gate IC303A causes a logic "1" at IC301C pin 3.

3. Preset 3 flip-flop IC301B resets. A logic "1" at pin 10 of "Or" gate IC302A causes a logic "1" at IC301B pin 11.

4. Preset 1 flip-flop IC301A is set. A logic "1" at pin 14 of IC301A causes a logic "1" at the Q output (pin 1) of IC301A.

With a logic "1" at the Q output of preset 1 flip-flop IC301A pin 1, several circuit functions take place:

1. The preset tuning potentiometer activates. The logic "1" at PCB pin 10 is connected to Section 9 PCB pin 4 where transistors Q612 and Q606 are switched ON, and the preset 1 potentiometer is activated.

2. Preset 1 LED indicator light is turned on. The logic "1" at PCB pin 1 (connected to Section 6 PCB pin 9) switches on transistor Q504. This allows current to flow through DS511 thereby providing the front panel indication.

3. Diode D301 is forward-biased ON, and places a logic "1" at pin 13 of "And" gate IC311B.

SCAN UP/DOWN. If the front panel SCAN UP touch button is touched, a positive-going pulse is generated in Section 6. The pulse is coupled thru Section 7 into Section 8 PCB pin 36. The positive-going pulse at pin 36 is directly coupled to pin 5 of "Or" gate IC306C. The output (pin 6) of IC306C is also at logic "1", and the following circuit functions take place:

1. The blanking circuit is activated. The output of "Or" gate IC306B goes to a logic "1" and toggles IC310B, the debounce time one-shot.

2. The main tuning knob flip-flop resets. IC312B pin 10 goes to a logic "1".

3. The presets 1 thru 4 flip-flops reset. "Or" gate IC304D (pin 3) goes to a logic "1".

4. The scan on/off flip-flop is set. With a logic "1"at pin 12 of IC307C, the Q output at pin 10 also goes to a logic "1".

5. The scan run/stop flip-flop is set. With a logic "1" at pin 6 of IC307D, the Q output at pin 9 also goes to a logic "1".

When PCB pin 36 goes positive, "Or" gate IC304B (pin 10) is at a logic "1". The logic "1" at pin 4 of the up/down scan flip-flop IC307A sets pin 2 (Q output) to a logic "1". This logic "1" will reverse-bias OFF Q301, and PCB pin 43 goes to −15 volts thru current-limiter resistor R302. The Q output of IC307A is connected to PCB pin 5, which in turn is connected to Section 6 to switch transistor Q508 ON, switch Q509 OFF, thereby illuminating the scan up LED, DS515.

If the SCAN DOWN touch button is touched, a positive-going pulse is generated, and PCB pin 37 would be at logic "1". The same circuit functions take place as in the scan up operation except that the "Or" gate IC304A (pin 11) goes to a logic "1" and resets the up/down scan flip-flop IC307A. The Q output at pin 2 of IC307A goes low and biases Q301 ON. With Q301 conducting, PCB pin 43 is at +15 volts potential. The logic "0" at pin 2 of IC307A is coupled to Section 6 thru PCB pin 5 to switch transistor Q508 OFF and Q509 ON, thereby illuminating the scan down LED DS516.

REMOTE SCAN ALL. When the rear panel switch S3 (REMOTE STATION SELECTOR) is in the SCAN ALL position and the remote control pushbutton is depressed, a positive-going pulse coming from Section 7 will be coupled to PCB pin 34. The output of "Or" gate IC306 goes to a logic "1" and the circuit functions as follows:

1. The frequency and signal strength displays are blanked.

2. The tuning knob flip-flop is reset.

3. The presets 1 thru 4 are reset.

4. The scan on/off flip-flop is set.

5. The scan run/stop flip-flop is set.

SCAN LIMITS. When the tuner scans to the top of the FM band, a positive-going pulse from Section 9

appears at PCB pin 8. This logic "1" at PCB performs the following:

1. Logic "1" at "Or" gate IC304A (pin 13) places a logic "1" at pin 3 of IC307A. This resets the Q output to a logic "0" and the tuner starts to scan down.

2. The logic "1" at both inputs (pins 1 & 2) of "And" gate IC311D produces a logic "1" at pin 4, the output of IC304C. This logic "1" forward-biases Q304 ON, and the collector connection is pulled to ground. Transistor Q305 is biased OFF and the relay contacts of K 303 are opened, thereby stopping the tuner from scanning up the FM band any further. NOTE: This only happens while maintaining finger contact with the SCAN UP touch button.

The identical circuit functions take place when the scan down limit is reached except "Or" gate IC304B and "And" gate IC311C are in the circuit.

SCAN ON/OFF. With the activation of SCAN UP, SCAN DOWN, or REMOTE SCAN tuning modes, pin 6 of "Or" gate IC306C goes high. The logic "1" from IC306C is directly coupled to pin 12 of IC307C (the SCAN ON/OFF flip-flop). This sets the Q output (pin 10) to logic "1", and the following takes place:

1. The front panel scan up or down LED is turned on. The logic "1" at PCB pin 6 is connected to Section 6 PCB pin 14 and switches ON transistor Q510. This allows current to flow through DS515 if the tuner is scanning up, or through DS516 if the tuner is scanning down, thereby providing front panel indication.

2. The scanning dummy load is activated. The logic "1" at PCB pin 16 is connected to Section 9 PCB pin 10 where transistors Q607 and Q601 are switched ON, and resistor R605 acts as a load for zener diode D601. The actual tuning voltage ramp for the scanning mode is produced by IC316, R339, and C315 of Section 8 and not in Section 9.

3. Diode D314 is forward-biased ON and this places a logic "1" at pin 13 of "And" gate IC311B.

4. The logic "1" is coupled thru R344 and R309 to the base of transistor Q302. Q302 is forward biased ON, transistor Q303 is reversed-biased OFF, and current flows through the coil of reed relay K301. The relay switch contacts close and the scan tuning voltage (at the junction of R339 and C315) is connected to PCB pin 18. This tuning voltage ramp starts the tuner scanning up or down the FM band. The tuning voltage at PCB pin 18 is connected to Section 9 PCB pin 12 and then on to the front-end circuitry in Section 3. When Q302 is switched OFF, current stops flowing through the coil of reed relay K301 and the switch contacts open.

SCAN STOP ONE-SHOT. The scan stop one-shot circuit stops the tuner from scanning past an FM station when one is reached. The tuner stops scanning when the RF signal strength of the station exceeds the signal strength setting of the front panel muting control.

IC309B is a monostable multivibrator whose output is used to reset the scan run/stop flip-flop IC307D thru "Or" gate IC305B. The unmute control signal from Section 4 PCB pin 31 is connected to PCB pin 27 in Section 8. PCB pin 27 goes to a logic "1" when an FM station is reached, and is connected thru R315 to IC309B pin 12. With pin 12 at a logic "1", pin 14 of IC309B is pulled low, and the output at pin 10 goes to a logic "1" (from its normal state of logic "0"). The logic "1" at pin 11 of "Or" gate IC305B causes a logic "1" to be at pin 7 of the scan run/stop flip-flop IC307D. This resets IC307D to the scan stop state, and the tuner stops scanning.

R315 and C308 form a filter to prevent noise from inadvertently tripping IC309B. Diode D320 discharges C308 quickly once an FM station has been reached. C307 and R314 form an RC time constant of very short duration to quickly return pin 14 of IC309B to a high state after the tuner has stopped on a station.

SCAN RUN/STOP. With the activation of SCAN UP, SCAN DOWN or REMOTE SCAN tuning modes, pin 6 of "Or" gate IC306C goes high. The logic "1" from IC306C is directly coupled to pin 6 of IC307D (the scan run/stop flip-flop). This sets the Q output (pin 9) to a logic "1", and the following takes place:

1. The lock lamp and the tuning lock circuit turns off. Pin 11 of "Or" gate IC306A is placed at a logic "1", and in turn, a logic "1" is at the output pin 10.

2. The logic "1" is coupled thru R311 and R312 to the base of transistor Q305. Q305 is forward-biased ON and current flows through the coil of reed relay K303. The relay switch contacts close and current is allowed to flow into pin 2 of IC316. This produces a tuning voltage ramp, and the tuner starts scanning.

LOCK LAMP DELAY. The lock lamp delay circuit prevents the lock lamp from becoming illuminated during the time the following occurs:

1. Finger contact with the MAIN TUNING knob.

2. Finger contact with the touch buttons of PRESETS 1 thru 4.

3. Finger contact with the SCAN UP and SCAN DOWN touch buttons.

4. When the tuner is scanning up or down the FM band.

5. When the remote control pushbuttons are depressed.

When pin 10 (the output of "Or" gate IC306A) goes high, diode D312 is forward-biased ON. This places a logic "1" at the input pins 3 and 9 of "Or" gate IC308B. "Nor" gates IC308B and IC308C wave-shape the signal. "Nor" gates IC308A and IC308D form a flip-flop circuit to keep diode D310 forward-biased ON during the above listed occurances 1 thru 5. The logic "1" at the cathode of diode D310 is connected to PCB pin 28, which in turn is connected to PCB pin 30 of Section 4. The logic "1" on PCB pin 30 of Section 4 keeps the lock lamp off. When the output of "Or" gate IC306A goes low, the charge on capacitor C303 prevents the input pins 3 and 9 (of "Or" gate IC308B) from going to a low state instantly. Resistor R305 slowly discharges C303 thereby providing the lock lamp delay.

MANUAL LOCK. "And" gate IC311A provides the means of keeping the lock circuit and lock lamp OFF when testing the tuner, or in cases when the station (the tuner is tuned to) has a deep fade to the point of losing the lock.

The logic "1" from pin 1 (Q output) of IC307B (main knob flip-flop) is directly coupled to pin 8 of "And" gate IC311A. If the lock switch S601C (Section 9) is in the OFF position, a logic "1" is coupled to pin 9 of "And" gate IC311A. With both inputs of "And" gate IC311A high, the output also goes high. This forward-biases D311 ON, which turns off the lock lamp. D315 is also forward biased ON, and pin 3 of IC313 is kept high, thereby turning off the lock circuit. NOTE: That the lock circuit can only be manually defeated in the knob mode.

SCAN TUNING VOLTAGE. IC316 is a special type MOS-FET integrated operational amplifier that has an input impedance of greater than one million megohms. This IC forms the heart of the scan ramp tuning voltage circuit. When the SCAN UP touch button (or REMOTE SCAN) is touched, reed relay contacts of K301 and K303 close, and the contacts of reed relay K302 open. With the contacts of K303 closed, a negative current source (formed by R335, R345, R2 and the −15 volt output of PCB pin 43) is connected to pin 2 of IC316 (the inverting input). IC316 will always try to keep both of the inputs (pins 2 & 3) at the same zero potential. This starts current flowing at pin 6 (the output of IC316) due to the fact that pin 3 is at zero potential. Resistor R339 limits the current and helps to provide circuit stability.

As current flows in the output of IC316, an extremely linear tuning voltage ramp is produced as capacitor C315 charges up. This tuning voltage ramp is connected thru the closed contacts of relay K301 to PCB pin 18. PCB pin 18 is connected to Section 9 PCB pin 12 and then onto the front-end circuitry in Section 3. When the SCAN DOWN touch button is touched, the same circuit functions take place except that a positive current source is connected thru Q301. Once an FM station is reached while scanning, the following things happen:

1. The scan run/stop flip-flop is reset. The unmuted signal from Section 4 trips IC309B (the scan stop one-shot) which in turn resets IC307D to the scan stop condition. This switches Q305 OFF, and the contacts of K303 open. This disconnects the current source from pin 2 of IC316 and current stops flowing in the output circuit. Capacitor C315 is no longer being charged, and due to its extremely low leakage, holds the scan tuning voltage ramp constant.

2. The lock circuit is activated. Any mistuning off the stations center frequency generates a voltage offset at the FM detector. This in turn is amplified by IC314 and fed to IC315, which produces a correction voltage. The correction voltage at pin 6 of IC315 is coupled thru R334 into the noninverting input (pin 3) of IC316. A positive or negative voltage forces IC316 to correct so that the inputs (pins 2 and 3) are at zero potential again. This current flowing in the output of IC316 corrects the voltage charge on C315 up or down. This alters the actual scan tuning voltage ramp so that the tuner is tuned to the center frequency of the FM station.

If the scan up, scan down or remote scan circuits are activated again, the scan run/stop flip-flop IC307D sets the Q output to a logic "1". This starts the scanning and locking process all over again until the next FM station is reached.

SCAN COMPARATOR. It is a desired feature to have the tuner start scanning from the frequency of the FM station (that the tuner was tuned to) when going from the MAIN TUNING knob or PRESETS to the scanning tuning mode. IC317 (a J-FET input operational amplifier) and its associated components provide this capability.

When the tuner is tuned by the MAIN TUNING knob or PRESETS 1 thru 4, relay contacts of K301 and K303 are open, and the contacts of K302 are closed. IC317 compares the tuning voltage of the main and

preset circuits to the scan tune voltage ramp. The tuning voltage established in Section 9 is connected to Section 8 thru PCB pin 18, and is coupled by R342 to pin 2 of IC317. Resistor R341 couples the scan tuning voltage from C315 to pin 3 of IC317. When a difference occurs between the tuning voltages at pin 2 and 3 of IC317, an output offset voltage is produced. This output voltage is limited by D329 and D328 to protect pin 2 input of IC316. Resistors R338 and R337, together with the voltage at pin 6 of IC317, form a positive or negative source for pin 2 of IC316. IC316 then forces the tuning voltage ramp at the junction of R339 and C315 to equal the tuning voltage set in Section 9. This action starts the tuner scanning from the frequency of the station tuned to (by the MAIN TUNING knob or PRESETS 1 thru 4) since the proper charge is stored by C315 to do so. R340 and C317 form a stabilizing feedback network for IC317.

SCAN SPEED UP. The varactor tuning diodes used in the front-end circuitry in Section 3 do not have a linear (voltage verses capacitance) relationship. As a result, the very linear scan tuning voltage ramp produced by the charging rate of C315 would cause the scanning speed of the tuner to slow down when scanning above 100MHz.

R336 couples the scan speed up control voltage from Section 10 (thru PCB pin 32) to the base of Q308. When the tuner is at or above 100MHz frequency, Q308 is forward-biased on. With Q308 switch ON, current flows through the coil of reed relay K304 and the contacts close. This shunts the current flowing to C315 around R335, and the increase in current flowing causes the charging rate of C315 to increase also, thereby speeding up the scanning speed of the tuner.

Front panel scan speed control R2 allows the user of tuner to varying the scanning speed by varying the amount of current flowing through it. R1 prevents having zero scanning speed.

TUNING LOCK CORRECTION. The tuning lock correction circuit consists of two operational amplifiers. The first op-amp IC314 is a logarithmic amplifier producing an output current proportional to the log of the input voltage. The second op-amp IC315 functions as a switchable gain low-pass filter.

The amplified composite detector output signal from Section 4 is connnected to PCB pin 29 and is coupled by R322 into IC314 (the log amp). The gain of IC314 is very high until the output voltage at pin 6 exceeds ± 1.3 volts, at which time diodes D323 and/or D324 are biased ON. If either diode is biased ON, negative feed-back is then applied to pin 2 of IC314. This reduces the gain and at the same time provides limiting action. Resistor R327 together with the output voltage from IC314 form a current source and are connected to pin 2 of IC315. IC315 serves a dual function: an integrator and low pass filter. C313 (which is in the feedback loop of IC315) removes the amplified audio signal coming from IC314. The gain of IC315 is switched from about 100dB down to less than unity gain depending whether or not Q306 (the N-channel J-FET) is conducting. Q306 and R326 are also in the feedback path of IC315. If you are tuned to a station, Q306 is switched OFF, and has several megohms of impedance between the source-drain connection. This allows little negative feedback around IC315 which then has a gain of about 100dB. With Q306 switched ON, the source-drain impedance drops down to several hundred ohms and increases the amount of negative feedback. This reduces the gain of IC315 to less than unity. The tuning lock correction voltage is connected to IC316 (scan tuning voltage ramp) thru R334 to correct for mistuning during the scanning operation. The correction voltage is also supplied to Section 9 thru PCB pin 17 to correct for tuning with the MAIN TUNING knob and PRESETS 1 thru 4.

FILTER OFFSET. The filter offset circuit provides a correction voltage to the tuning lock circuit to compensate tuning when the SUPER NARROW filter is selected. The 10.7MHz filters (used in Section 3) have different tolerances; ±30kHz for ceramic filters FN202 thru FN206, and ± 2kHz for the crystal quartz filter FN201. Due to the extremely selective supper narrow crystal filter, a tuning offset correction may be needed to center the FM station (for the crystal filter) in order to provide the lowest distortion audio output.

If the front panel IF selectivity switch S1 is in the NARROW position, PCB pin 20 is at +15V which will keep the gate of Q307 (P-channel J-FET) positive. With the gate positive, Q307 is switched off. Resistor R328 and R329 limit the current flowing in the gate of Q307. C312 provides filtering for the +15 volts.

When S1 is placed in the SUPER NARROW position, the gate of Q307 goes to ground, and Q307 is switched on. Potentiometer R331 allows a positive or negative voltage offset to correct for the actual center frequency of the quartz crystal filter. The filter offset correction is connected to pin 2 of IC315, and the lock circuit then corrects for the optimum tuning point. Diodes D330 and D326 limit the offset to ±0.4 volts.Resistor R330 limits the current flowing through Q307.

LOCK INHIBIT. The lock inhibit circuit consists of operational amplifier IC313 and N-channel FET Q306. IC313 functions as a deviation detector and has a range of ±500kHz so the lock circuit will not lock onto a strong adjacent signal when tuned to a

weak station.

The amplified composite detector output signal is connected to PCB pin 29 and is coupled by R317 to the junction of diodes D321 and D322. If the tuner is tune off station, the detector in Section 3 generates an offset voltage. If the mistuning voltage is greater than ± 0.6V, diodes D321 or D322 will conduct. When either diode conducts, the output (pin 6) of IC313 goes positive. With a positive voltage at pin 6, the gate of Q306 goes positive. With the gate of Q306 positive, Q306 is switched ON, and the impedance between the source-drain connection is several hundred ohms. This reduces the gain of IC315 to less than unity and the correction voltage is reduced to near zero. Resistor R324 limits the current flowing from IC313, and R325 limits the current flowing in the gate circuit of Q306. D325 conducts to prevent the gate of Q301 from going beyond 0.6V positive.

If the MAIN TUNING knob, PRESETS 1 thru 4 or the SCAN functions are activated, the output of "Or" gate IC306A (pin 10) goes high. This forward-biases D316 ON, and pin 3 of IC313 also goes high to produce a positive voltage at pin 6 of IC313. This action disables the tuning lock circuit during tuning.

SECTION 9 · TOP COVER CONTROLS, BAND LIMITS, MAIN & PRESET TUNING

This section contains three major functions: tuning voltage (which is used by the front end), scan up band limit (which prevents tuning above 108.1MHz) and scan down band limit (which prevents tuning below 87.4MHz), and the top cover switches and controls.

TUNING VOLTAGE REGULATION. D601 is a special temperature-compensated zener diode which provides an extremely stable voltage reference of +33V for tuning the varactor diode front end. 3mA of current from the constant current source in the power supply helps to maintain proper zener diode action.

MAIN & PRESET TUNING. The main tuning knob and presets 1 through 4 function in the same manner, therefore only the main tuning circuit will be described. When the MAIN TUNING knob is touched, the knob flip-flop (IC307B in Section 8) is toggled to logic level "1" and is coupled through R611 to switch on Q608, which in turn biases on Q602 thus activating the main tuning knob potentiometer R610 which permits the tuning voltage to be controlled by R610.

TUNING VOLTAGE LIMITS. The maximum tuning voltage is established by the setting of R601 (top of band adjust) and the minimum tuning voltage is set by R602 (bottom of band adjust). Resistor R609 limits the current through Q602; D604 couples the DC tuning voltage to the tuning buss line connected to Pins 12 and 13. Diodes D605 through D608 are all reverse biased to prevent the preset potentiometers from adding to the main tuning potentiometer voltage. Capacitor C601 is a filter bypass for D601, and C606 bypasses the 19kHz touch signal (which is present on the main tuning control) from becoming rectified by D604 and adding to the tuning voltage.

LOCK CORRECTION. The lock circuit tuning correction voltage (±1.4V) from Section 8 is connected to Pin 11 and is either added to or subtracted from the +33V in order to correct for any mistuning or circuit drift of the front end. Diodes D602 and D603 clamp the correction voltage to a limit of ±1.4V which is sufficient to correct for one whole megahertz either side of the desired frequency.

Transistor Q601 and resistor R605 act as a dummy load for the tuning voltage supply when the tuner is in the scan up or scan down mode (the actual scan tuning voltage is generated on Section 8 for scaning up or down).

SCANING LIMITS. To insure against scanning above or below the FM band, two comparator circuits are used. Resistors R632, R633, R634, R635 and R636 form a voltage divider to establish the upper and lower limits. IC601 is normally generating a large voltage offset at its output due to the fact that R633 is adjusted to provide +26.1V at Pin 3 and Pin 2 has less than +26.1V. When the top of the FM band is reached, both Pins 2 and 3 have the same voltage, and the voltage at Pin 6 of IC601 drops to about 1V thus switching off Q613 and allowing +15V through R641 to the scan up limit out at Pin 2. The scan down limit is generated in an identical manner by IC602 and Q614, and provides a +15V at Pin 9 at the down limit.

The last major portion of Section 9 consists of switch S601A, B, C, D, E which provides control of the RF preselector circuit, switching between two RF sources, turning the lock circuit on and off, and selecting the correct FM de-emphasis curve. Signal strength adjust R643, together with R645, R646 and R644, provides the means of adjusting the signal strength LED display maximum point to show relative signal strength in both strong and weak RF reception areas.

SECTION 10 - FREQUENCY COUNTER ASSEMBLY

This section contains frequency dividers, counters and a stable 200kHz crystal oscillator. Together they provide the necessary circuitry so that a digital LED readout can display the actual frequency of the tuned station.

200kHz OSCILLATOR. The 200kHz crystal oscillator circuit is made up of Q101, Y101, IC111A, L101, C107, C108, C106, R114 and R113. IC111B shapes and inverts the signal to produce a 200kHz square wave. From there, IC112A and B (Dual J-K Flip Flop) divides by four to 50kHz and is direct coupled to IC113 (a 4 bit binary counter) which divides it by 16, then on to another divided by 16 (4 bit binary counter) IC114. At the output of IC114 (Pin 12) the frequency is 195.3Hz and if fed into IC115 which divides to produce simultaneous 48.9Hz, 24.5Hz and 12.2Hz frequency outputs.

BUFFER AMPLIFIER. The front end oscillator output is coupled by C101 to IC101A, the first of a three stage buffer amplifier (IC101A, B and C) made from emitter coupled logic circuits baised on as amplifiers, to increase the amplitude of the oscillator signal. Components R101, R102, C104 and C105 form a noise filter to attenuate any noise accompanying the front-end oscillator signal.

ECL DIVIDER. IC102A and B (dual type D Flip-Flop) form a divide by four and R109, R110, R111 and R112 are pulldown resistors to bias IC102A and B at ECL levels. The divided signal from IC102A and B is at emitter-coupled logic levels and is logic level shifted up to TTL logic levels for use in the rest of the frequency counter circuits.

ECL CONVERSION. IC103B is a bias source for IC103A so that the input (Pin 1) of this "Nand" gate is kept active. When the small ECL level from IC102B (coupled by C110) is applied to Pin 1 of IC103A, the output at Pin 3 changes state, thus converting ECL to TTL logic levels. C111 provides stability for IC103B, and L102C prevents the AC coupled ECL levels from reaching IC103B. The output of IC103A is wave-shaped and inverted by IC103C and fed directly into IC104A.

MAIN COUNTER. IC104A and B (dual J-K Flip-Flop) samples the divided front-end oscillator signal for a duration of 40.98mS by the positive going gating pulse from IC115 Pin 12 and divides the input frequency by a factor of 4. The output of IC104B is coupled to IC106 (4 bit binary counter) which divides by 16. The output of IC106 drives IC107 which also divides by 16, however it is preloaded to start counting from the BCD number 7. The reason it starts counting from the BCD number 7 is to allow the 100 kilohertz digit readout (the number to the right of the decimal point) to indicated the desired frequency from 50 kHz below to 50kHz above the actual frequency.

In order to have the digital frequency display show the stations frequency instead of the oscillator frequency (which is always 10.7MHz higher), the following three counters IC108, IC109 and IC110 are preloaded to subtract the 10.7MHz "IF" offset from the actual frequency. This subtraction is accomplished by adding 89.3 (tens compliment) of 10.7 to the counted frequency.

PRELOADED COUNTERS. IC108 (the fractions counter) starts counting from its preloaded number of 3, IC109 (the units counter), starts counting from its preloaded number of 9 and IC110 (the tens counter) starts counting from its preloaded number of 8. The outputs of IC108, IC109, IC110 (decade counters) are encoded to BCD code and are driven by IC505, IC504, IC503 respectively (latch, decoder, LED driver) in Section 6.

GATING PULSES. "Nand" gate IC111C, IC103D, IC111D invert the outputs from IC115 (Pins 9, 2 and 12) and couple them into IC105A and B ("Nand" gates). IC105A and B then combine their various inputs to produce two 6mS gating pulses which are displaced in time from each other.

DISPLAY UPDATING. When the positive going-gating pulse of 40.98mS (IC115 Pin 12) toggles the J-K inputs of IC104 to an "ON" condition, all the following dividers and counters also start counting. When the 40.98mS gating pulse goes negative, all dividing and counting stops. 15mS after all counting stops a negative going 6mS duration pulse (IC105B Pin 8) is sent to the latches in IC503, IC504, IC505 (Section 6), the BCD information from the three decade counters is then transferred to the decoders in IC503, IC504 and IC505, and finally the display is updated. 4mS later, another negative going 6mS duration pulse (IC105A Pin 6) is used to reset IC104, IC106 through IC110 so they can start counting all over again when the 40.98mS gating pulse at IC104A (Pin 2 and 3) goes positive again.

REPACKING INSTRUCTIONS

In the event it is necessary to return a unit to McIntosh Laboratory for service, the MR 80 must be packed exactly as shown below. It is not necessary to return the shelf brackets, although their position in the carton is shown.

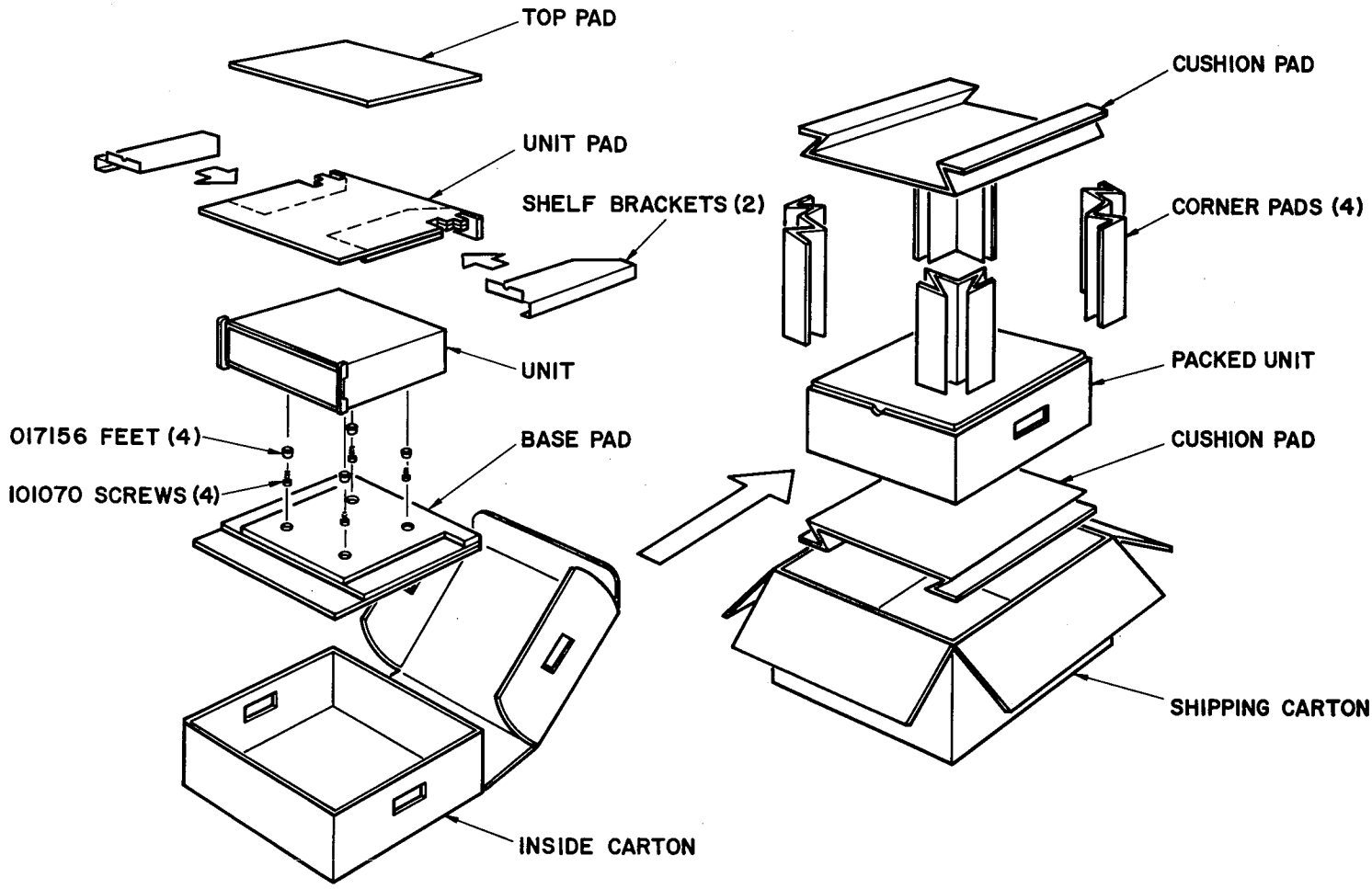
The plastic feet must be attached to the bottom of the MR 80 so they will locate the unit in the four holes of the base pad.

If a shipping carton is needed, please call or write the Customer Service Department of McIntosh Laboratory. Order using the part numbers below:

QTY	PART NUMBER	DESCRIPTION
1	045617	Shipping Carton & Pads
4	017156	Plastic Feet
4	101070	Mounting Screws for Feet

Use the original shipping carton only if all pads and cartons are in good serviceable condition.

SHIPPING CARTON ASSEMBLY



McIntosh

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