

Timer Counter
TC4A

Instruction Manual



ADVANCE

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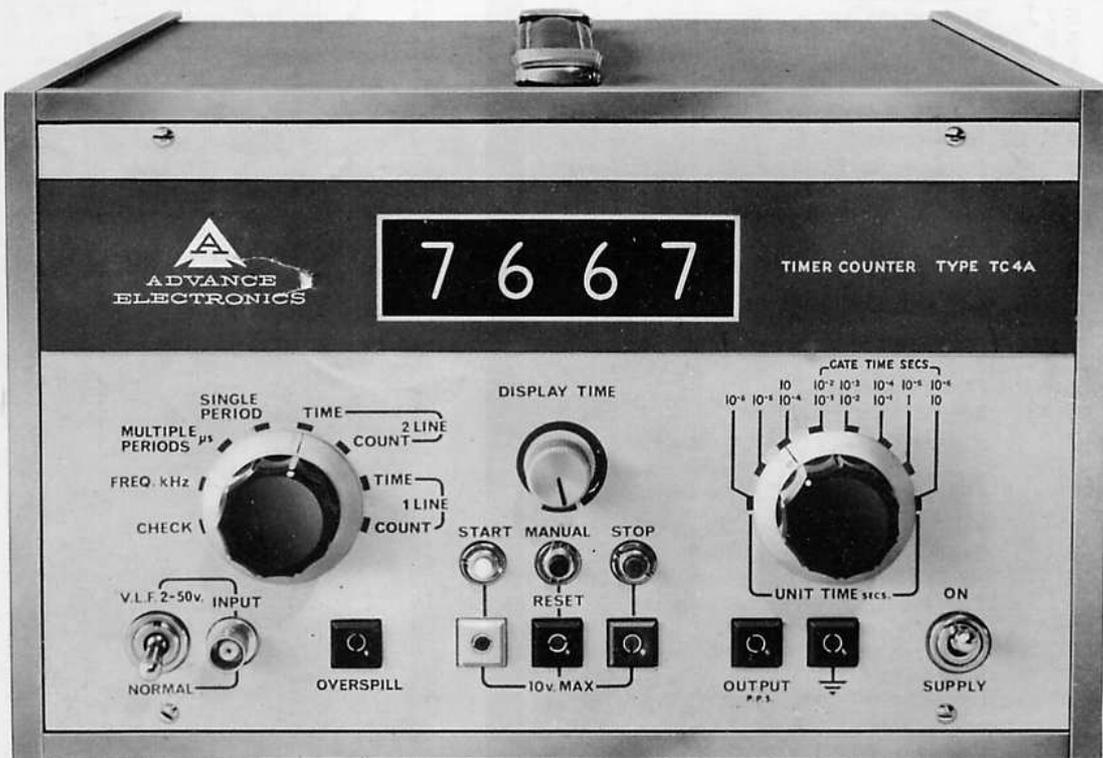
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The Time Counter TC4A is a high grade instrument for accurate measurement of frequency, period, time and for counting regular or random pulses at a maximum rate of at least five million per second. The display has four figures and a decimal point which are in-line and easy-to-read with bright clear figures. No difficulty is experienced in reading the display over a wide angle. For frequency measurement the display is always indicated in kilohertz with an automatically positioned decimal point.

All operating controls are mounted on the front panel, together with the INPUT, OUTPUT, START, STOP, RESET, OVERSPILL and earth sockets. The external standard socket (EXT. STANDARD) is located at the rear of the instrument. When the case is removed, the fuses are accessible at the rear and adjustment can be made for the alternative supply voltage range by use of the interlocked switch.

To provide easy access to all internal components, a system of unit construction has been adopted. The exceptionally compact and lightweight design has been achieved by making the maximum use of transistors and printed circuit boards. The circuit is divided into sub-units each of which is constructed on a separate printed circuit board. The internal frequency standard is an oven controlled 1MHz crystal oscillator which also provides, through decade frequency dividers, output timing pulses at any one of eight standard frequencies. Self-checking facilities are available for testing the operation of the two counter chains and the display.

An optional facility is an output to operate the Kienzle D11E printer, this is a parallel entry type in which all the figures in a display are printed simultaneously.



Display

Four in-line neon indicators with decimal points.

Display Accuracy ± 1 count \pm accuracy of standard.

Display Resetting

Automatic Under control of display timer between approximately 0.3 to 7 seconds for all events longer than 50ms.

Manual By operation of front panel push button.

Electrical Using positive pulses with amplitude greater than 5V, and width greater than 20 μ s.

Frequency Measurement

Range 0 to at least 5 MHz.

Gate times 0.001, 0.01, 1 or 10 second. Decimal point automatically positioned for display in kHz.

Sensitivity

NORMAL input 10 Hz to 5 MHz, sinusoidal signal from 100 mV rms. Maximum input 250V rms up to 100 kHz and 10V rms up to 5 MHz.

VLF input 0 to 10 kHz signals between 2V and 50V.

Input Impedance

NORMAL input approximately 100 k Ω shunted by 30 pF.

VLF input approximately 5 k Ω .

Period Measurement

Single period A single input cycle in range 1 ms to 10⁴s measured with selected timing pulses of 10⁻⁶, 10⁻⁵, 10⁻⁴, 10⁻³, 10⁻², 10⁻¹, 1 or 10 per second.

Multiple period 10, 10², 10³, 10⁴, 10⁵ and 10⁶ periods measured with 1 μ s pulses. Minimum period 10 μ s using 10³, 10⁴ and 10⁵ periods, 100 μ s using 10² periods and 1ms using 10 periods.

Period Sensitivity As for frequency measurement.

Time Measurement

Unit time pulses 1 μ s to 10 seconds in decade steps. Maximum period that can be displayed is 10⁵ seconds (approximately 28 hours).

Operation One or two line operation by use of push buttons when totals can be integrated, or using external signals (see under Sensitivity).

Sensitivity Positive pulses between 2 and 10V peak. Reference to earth is required. For 2V sensitivity a rise time of 0.5–1.5 μ s required. Slower rise time pulses must be of larger amplitude.

Output Timing Pulses

Decade divisions between 10⁶ per second and one pulse per 10 seconds. Nominal 5V peak positive going, from 10k Ω source. Mark/space ratio approximately 3:2. Pulses not available in multiple periods function.

Counting

Range 1 to 9999, regular or random pulses.

Operation One or two line operation by use of push buttons or external signals.

Sensitivity As for frequency measurement.

Frequency Standard

Internal 1 MHz crystal oscillator, oven controlled at +65°C.

Setting accuracy 1 part in 10⁶ at +25°C.

Stability ± 5 parts in 10⁶ from 0 to +40°C.

External Any sinusoidal signal from 500 kHz to 1 MHz between 1.5V and 10V rms or a suitable pulse signal having a width 1 to 10 μ s and repetition frequency from 1 kHz to 1 MHz. A 400V pk. blocking capacitor is fitted in series with the input jack. For details of Advance Off-Air Standard OFS1, see separate leaflet.

Check Facility

Crystal derived 10 kHz counted for 10 seconds to check both dividing chains. Display shows 0000 ± 1 .

Counter Overspill

Output of lowest LF counting decade appears at OVERSPILL socket as a nominal 1:1 pulse of approximately 6V from a nominal 1k Ω source. This output must not be terminated in less than 20k Ω as it is a voltage source only.

Printer Output

An output socket is provided on the rear panel to operate the Kienzle D11E printer.

Operating Temperature Range

0 to +40°C.

Accessories Supplied

One 50 Ω BNC/BNC connector PL43; one 50 Ω BNC/clip connector PL44; three 4mm wander plugs, red, white and black; one miniature jack plug, Part No. 448; one Instruction Manual Part No. 20344.

Power Supply Requirements

100 to 125V or 200 to 250V, 45 to 65 Hz, 30VA nominal.

Dimensions

11" wide 7½" high 13" deep (28×19.1×33 cm).

Weight

15¾lb (7.14kg).

Finish

Light blue case with light grey front panel having a dark grey band.

3.1 GENERAL

When despatched from the factory the counter is normally set to operate from a nominal 240V supply. To operate from a nominal 110V supply, change the switch at the rear of the instrument (see Fig. 16). The ventilation holes of the case must be kept clear at all times.

3.2 INITIAL ADJUSTMENT

- Check that the voltage switch is correctly positioned for the supply used.
- Switch ON.
- The RESET button must always be pressed after switching ON or after moving the selector switch to a different function.
- Carry out the self-checking procedure detailed in paragraph 3.7.
- Although the crystal oven begins to cycle off and on within 20 minutes of switching on the counter, the maximum standard accuracy is only achieved after a period of approximately one hour. At an ambient temperature of +25°C an accuracy of 3 parts in 10^6 is obtained within approximately 20 minutes.

3.3 FREQUENCY MEASUREMENT

Fig. 1 shows a block schematic diagram of the arrangement of the counter circuits for the purpose of frequency measurement. The amplitude of sinusoidal input signals should be at least 100mV rms and not greater than 250V rms up to 100kHz and 10V up to 6MHz. If the input consists of short unidirectional pulses, the pulse polarity must be positive and must not exceed 400V pk.

The GATE TIME SECS. switch shows five gate times: 10^{-3} , 10^{-2} , 10^{-1} , 1 and 10 seconds. In each case the display indicates the frequency in kHz with an automatically positioned decimal point. The first position 10^{-3} is used to find the first digits at frequencies above 1kHz, and with a short DISPLAY TIME, gives an almost continuous indication of frequency.

Due to the possible error of \pm one count, the absolute accuracy (ignoring crystal accuracy) becomes progressively less as the input frequency is decreased. The best accuracy at 10kHz on 10 sec. GATE TIME is thus $\pm 0.001\%$ (10 parts per million).

For greater accuracy at frequencies below 100kHz it is advisable to select period measurement. On MULTIPLE PERIODS $\times 10^3$ the accuracy achieved at 50kHz is $\pm 0.005\%$ and below 50kHz the accuracy increases progressively, neglecting any trigger point errors. These trigger point errors can be as much as 0.3% per period. Obviously the larger the number of units registered on the decades the less significant becomes the ± 1 count error. The counter can be overfilled and provided the lost digits are known, greater accuracy can be achieved by increasing the number of periods measured.

Repetitive readings are obtained when the DISPLAY TIME control is not fully counter-clockwise. The length of time for which a reading is displayed depends on the setting of this control and can be varied between 0.3 and 7 seconds. Longer display times may be achieved by switching to MANUAL, i.e. DISPLAY TIME control fully counter-clockwise. It is then necessary to use the RESET push-button, or the electrical reset

on the front panel, in order to set the counter to zero and initiate a counting period. At the end of the counting period the indicators display the frequency until the push-button is again operated. When AUTOMATIC is selected, it is also necessary to press the RESET button immediately after switching on, to ensure the commencement of the display time cycle.

3.4 PERIOD MEASUREMENT

(a) *Single Period.* To obtain an accurate determination of the lower frequencies it is better to measure the period of the signal, that is, the time elapsing between two consecutive zero transits of the signal in the positive direction. This is performed when the selector switch is set to SINGLE PERIOD. A block diagram of the arrangement is shown in Fig. 2. The indicators show the time period determined by the setting of the UNIT TIME SECS. switch, and it is necessary to take the inverse of this reading to obtain the frequency. For example, using microsecond units (UNIT TIME SECS. 10^{-6}), a reading of $200,000 \pm 1\mu\text{s}$ gives a frequency of $5\text{Hz} \pm 0.0005\%$ assuming a constant zero transit of the signal, i.e. no trigger point error. The first two digits may be found using millisecond clock units (UNIT TIME SECS. 10^{-3}). Frequencies below 10Hz must be switched to the V.L.F. input and must be between +2V and +50V pk. amplitude. The trigger point error for a single period at the lowest limit of signal input level may be as great as 5%; this is usually due to noise or to spurious signals that are not related harmonically, such as hum. Greater accuracy can be obtained by increasing the level of the input signal and typically, with 5V peak input at 15Hz, the error should be no greater than 0.1%.

(b) *Multiple Periods.* The time indicated on the counter is always in microsecond units and is the time elapsing between the first positive-going zero transit of the input signal and a selected subsequent transit. The selection of the latter transit is made according to the PERIODS selected. A block diagram is shown in Fig. 3. Selected transits may be the tenth, hundredth, etc., up to the millionth. The period of frequencies above 100kHz cannot be measured owing to limitations in the operating speed of certain circuits involved. In the $\times 10^4$ position of the UNIT TIME SECS. switch, the accuracy with an input frequency of 50Hz, ignoring the trigger point errors, will be $\pm 1\mu\text{s}$ in $2 \times 10^8 \mu\text{s} \pm$ standard accuracy. Note that here the first six digits will be lost (carried over) and must be assumed. The first four digits can be found by selecting SINGLE PERIOD and by using 10^5 clock units.

3.5 TIME MEASUREMENT (Fig. 4)

When the selector switch is at TIME, the counter will measure the time interval between two pulses applied to the START and STOP sockets, or alternatively between the operation of the START and STOP push-buttons. It should be noted that when 2-LINE working is selected, the start-stop pulses cannot have a common course, that is, each pulse must be fed only to its appropriate socket.

The pulses should be positive going to initiate the start-stop circuit and should have a terminal voltage of 2V to 10V. The rise time must be between $0.5\mu\text{s}$

and $1.5\mu\text{s}$ for a 2V sensitivity. Pulses having a rise time greater than $1.5\mu\text{s}$ need to be of greater amplitude for satisfactory operation. If the START-STOP pulses are derived by switching d.c. supplies, it will be necessary to discharge the START and STOP input capacitors before a repeat measurement can be carried out.

Pulses having a common source should be fed into the START socket only, and 1-LINE working should be selected: the pulses should meet the normal input requirements for the START socket.

The units of time registered on the indicators may be selected, by means of the UNIT TIME SECS. switch, to be $1\mu\text{s}$, $10\mu\text{s}$, $100\mu\text{s}$, 1ms , 10ms , 100ms , 1 or 10sec . The smallest time that can be practically measured is 1ms to an accuracy of $\pm 1\mu\text{s}$, and the longest time that can be displayed is 10^5 sec. (approx. 28 hours) to an accuracy of ± 10 sec. \pm the crystal accuracy.

It should be noted that when the start-stop is initiated by means of pulses, the electronic circuits in the start-stop circuits will require to be reset. This can be done manually by means of the push-button, or automatically at the end of the display time. In either case the readings will then revert to zero. However, when the start-stop is initiated by means of the push-buttons it is possible to add a number of time periods to the first. This occurs automatically as the START and STOP push-buttons are operated successively for each period. The counter can then be made to indicate the total of a number of time periods.

3.6 COUNTING (Fig. 5)

The operation of counting is similar to that for time measurement except that instead of timing pulses being fed to the counting system, pulses of external origin, which may be random in nature, take their place. The selector switch must be set to COUNT and the indicators will then show the total number of pulses fed to the input socket either between start and stop pulses, or between the operation of the START and STOP buttons. In the latter case, as in time measurement, the total of a number of such operations may be added.

3.7 SELF-CHECKING FACILITY (Fig. 6)

When any doubt exists as to the correct functioning of the instrument, the selector switch should be set to CHECK and the DISPLAY TIME control turned fully clockwise. Under these conditions, all circuits are brought into use, and test signals derived from the 1MHz crystal oscillator are fed to both counter chains. A series of $100\mu\text{s}$ pulses is fed to the counting system for a period of 10 sec., as determined by the timing pulse generator. At the end of this counting period, if the equipment is functioning correctly, the counter will indicate 0000 ± 1 count (i.e. 9999, 0000 or 0001) for a display period of seven seconds, and then resume counting.

Self-checking may be carried out immediately the counter is switched on as this facility is not affected by the warming up period of the crystal oven.

3.8 COUNTER OVERSPILL FACILITY

The output of the display counter (LF decade) is available at the counter OVERSPILL socket, at the front panel of the instrument, and provides a means of obtaining additional digit values, i.e. a means of effectively extending the normal display to the left. The output signal consists of a nominal 1:1 pulse of

approximately 6V amplitude suitable for driving a high impedance circuit, i.e. not less than $20\text{k}\Omega$. This output must not be shorted to earth.

The overspill output can be displayed on an oscilloscope or can be used to operate an additional electronic counter or mechanical indicator after suitable shaping and amplification.

3.9 PRINTER OUTPUT FACILITY

This facility is fitted to timer counters as an optional accessory and enables them to operate the Kienzle D11E printer. This is a parallel entry type in which all the figures in a reading are printed simultaneously. To operate the printer it is only necessary to plug it into the PRINTER socket at the rear of the counter.

A description of the printer and its detailed mechanical and electrical operation will be found in the printer handbook. The adaptor circuit, however, is described in paragraph 4.9.

The principle of operation is that a row of print-wheels, which are engraved with the figures 0 to 9, are rotated at the same time as ten pulses are fed to the input of each decade in the counter. The output "carry" pulse from each decade is taken back to the printer and locks the print-wheel, preventing any further rotation.

For example, suppose that the counter indicates the number 7 in a particular decade. The associated print-wheel starts from 0 and is rotated backwards. A pulse is generated by the printer as the wheel goes from 0 to 9 and this is used to step the decade forward from 7 to 8. A second pulse is generated as the wheel moves backwards from 9 to 8, stepping the decade from 8 to 9. A third pulse is generated by the printer as the wheel moves from 8 to 7, and this steps the decade from 9 to 0. An output "carry" pulse from the decade occurs as it goes from 9 to 0 and this pulse is fed back to the printer to energise a solenoid and prevent any further rotation of the print-wheel, which is thus locked in the 7 position. The remainder of the ten pulses from the printer continue to be fed to the decade, which therefore returns to its original state and indicates 7 again on the counter display.

All the other decades in the counter have been stepped at the same times as the one described above, so that all the print wheels are set to the required numbers simultaneously. The print wheels are then forced by springs to print the result on the paper.

3.10 SPECIAL APPLICATIONS

(a) General

Counters are exceedingly versatile instruments, and a few unusual applications are mentioned so that the facilities provided by the TC4A can be appreciated and used to the full. The basic facilities provided are counting, measurement of time, frequency and period: all of these facilities are extremely accurate, and because of this, any action which can be converted into a suitable electrical analogue can be very accurately measured.

For example, the velocity of almost any moving part, missile, or vehicle can be measured over a fixed distance by generating start and stop pulses at the commencement and completion of the distance, and timing the interval between these two pulses. The time interval between the energisation of a relay coil and the operation of its contacts can be measured, and

the outputs from radio-activity detectors such as Geiger-Muller tubes and scintillation probes can be readily counted.

The use of the V.L.F. input effectively extends the frequency range of the counter from the normal minimum of 10Hz, virtually down to d.c. thus opening a new realm of applications in the measurement of long-period variables. Apart from the possibility of using an external frequency standard for greater accuracy, the choice of a different external frequency enables the counter to give readings based on different units. For example when using the counter as a tachometer it is preferable to read r.p.m. x10, and not r.p.s. therefore an external standard of

$$\frac{10^6}{6} \text{ Hz could be chosen.}$$

Four special applications of the TC4A are selected for description in the following paragraphs.

(b) Phase Measurement

Measurement of phase requires the generation of a positive pulse to the START socket from the reference phase at the moment of zero transit, and a similar pulse to the STOP socket from the phase requiring measurement. The instrument should be set for TIME measurement, usually with microsecond time units.

Once the period of the input frequency has been accurately measured, the phase lag in degrees may be found from:

$$\frac{\text{Time } (\mu\text{s}) \times 360^\circ}{\text{Period } (\mu\text{s})} \phi \text{ lag.}$$

Assuming the generation of the start and stop pulses to be accurate, the phase can be calculated to 1° accuracy ($\pm 1\mu\text{s}$) with a frequency whose period is $360\mu\text{s}$, i.e. 2780Hz.

(c) Tachometry

For this purpose, a means is required of producing a pulse or sine wave whose p.r.f. or frequency bears a fixed relationship to the speed of the shaft in hertz per second. These devices can be photoelectric, magnetic or capacity pick-ups.

In general the frequencies to be measured in tachometry will be lower than 50,000Hz, so that for extreme accuracy the period and not the frequency should be

measured. Shaft speeds are usually quoted in r.p.m. so that a conversion is necessary by either method, unless an external standard of

$$\frac{10^6}{6} \text{ Hz}$$

is used as shown above. If the period is measured, better accuracy is obtained by producing only one pulse output for every shaft revolution. If the frequency is measured, greater accuracy is obtained by producing a large number of signals at each revolution of the shaft. A magnetic transducer and a 60 tooth wheel will give a reading in r.p.m. without conversion.

(d) Torque Measurements

As an extension to the previous two applications, and in view of the improved accuracy of phase measurement at low frequencies, comes the measurement of torque.

A torque bar of known characteristics should be utilised, which, under conditions of zero torque, produces coincident pulses or pulses of known angular displacement at either end. These are the start and stop pulses. The period of revolution is first measured using either the start or stop pulse only, then the time separating the two pulses under torque. The phase angle may be calculated and a correction made for any displacement angle to find the angular twist of the torque bar; from this the torque may be calculated.

(e) Viscosity Measurement

The viscosity of a fluid may be measured by allowing a ball to roll down an inclined tube which has been filled with the fluid under test. The velocity of the ball at low roll speeds and under laminar flow conditions is then a measurement of viscosity. Contacts can be provided at each end of the tube, and the instrument calibrated for temperature and inclination.

(f) Frequency Measurement To 100 MHz

The Advance Frequency Divider TCD100A is available to extend the range of the TC4A to 100MHz, by providing division factors of 20 and 100. Additionally, the TCD40 provides similar facilities up to 40MHz, with division factors of 100, 40, 10, 4 and 1.

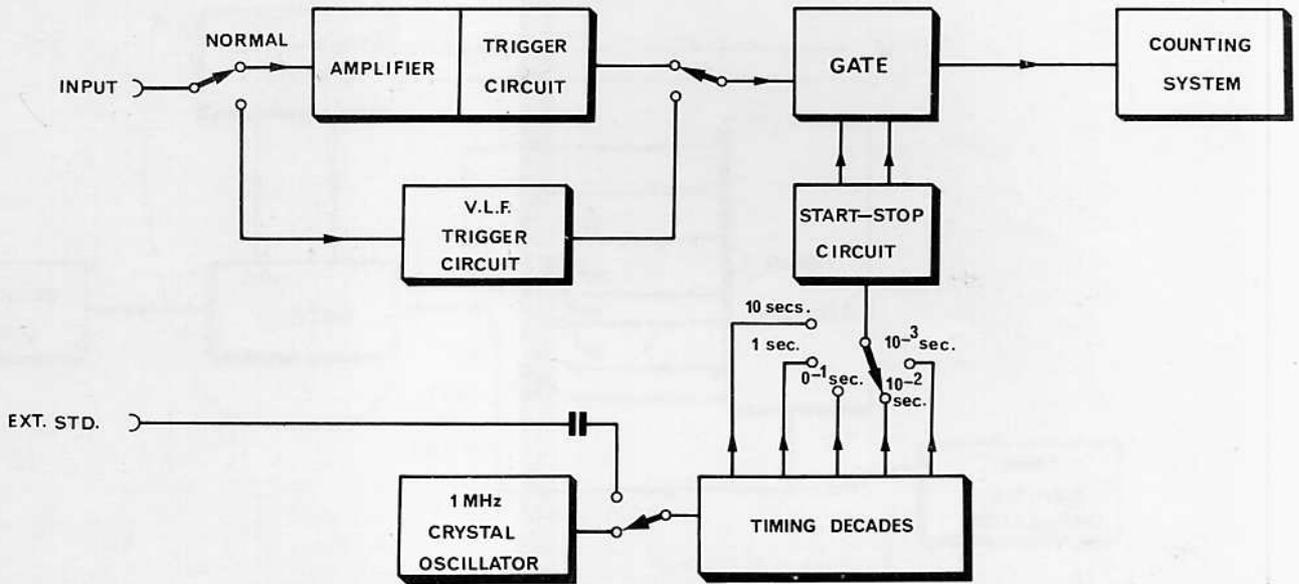


Fig. 1 Frequency Measurement

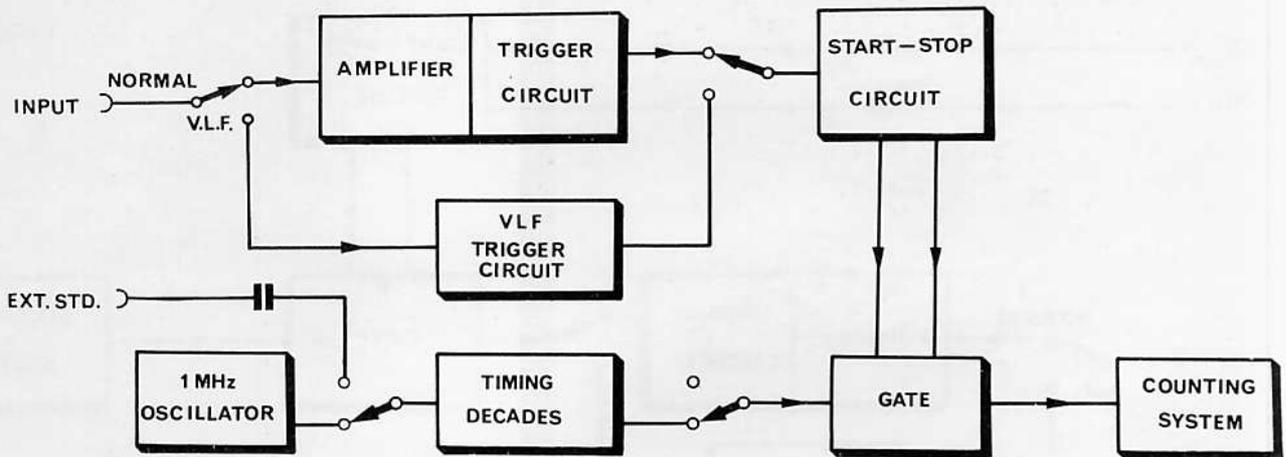


Fig. 2 Single Period Measurement

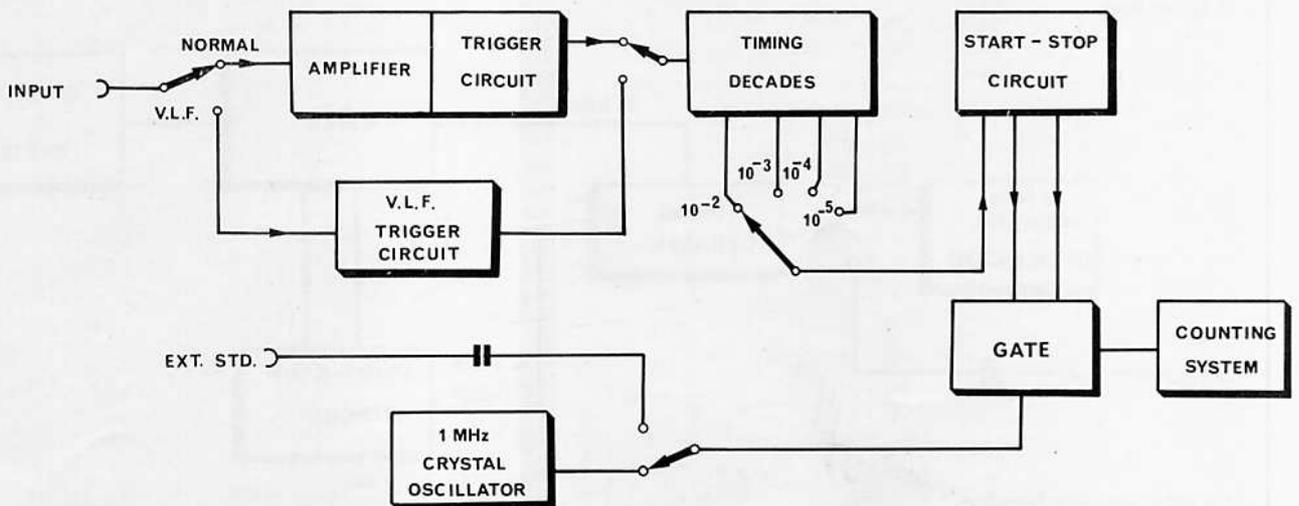


Fig. 3 Multiple Period Measurement

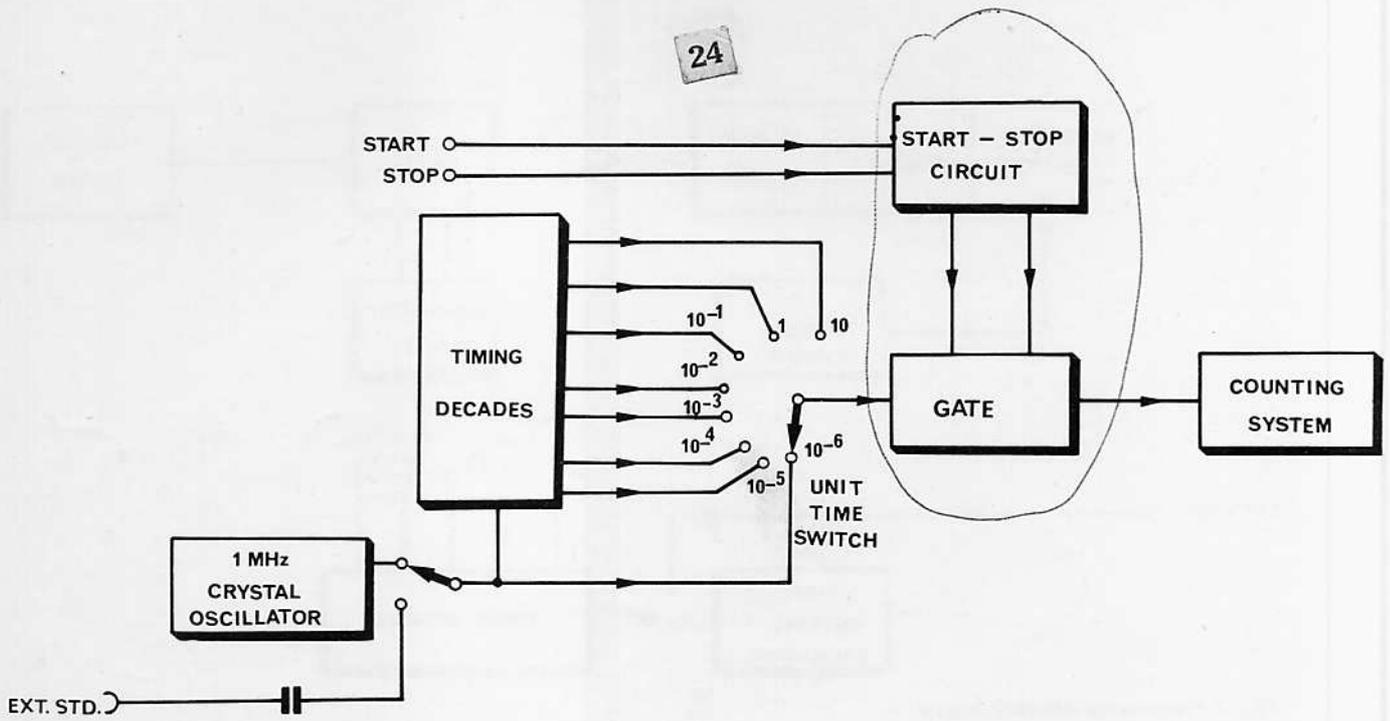


Fig. 4 Time Measurement

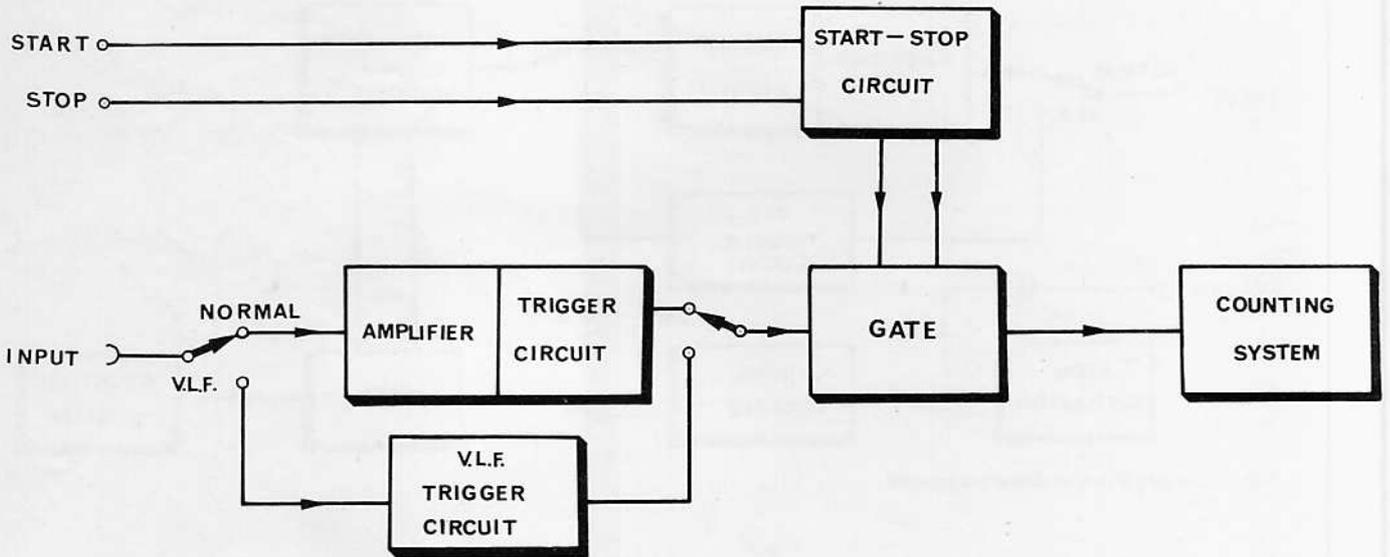


Fig. 5 Counting

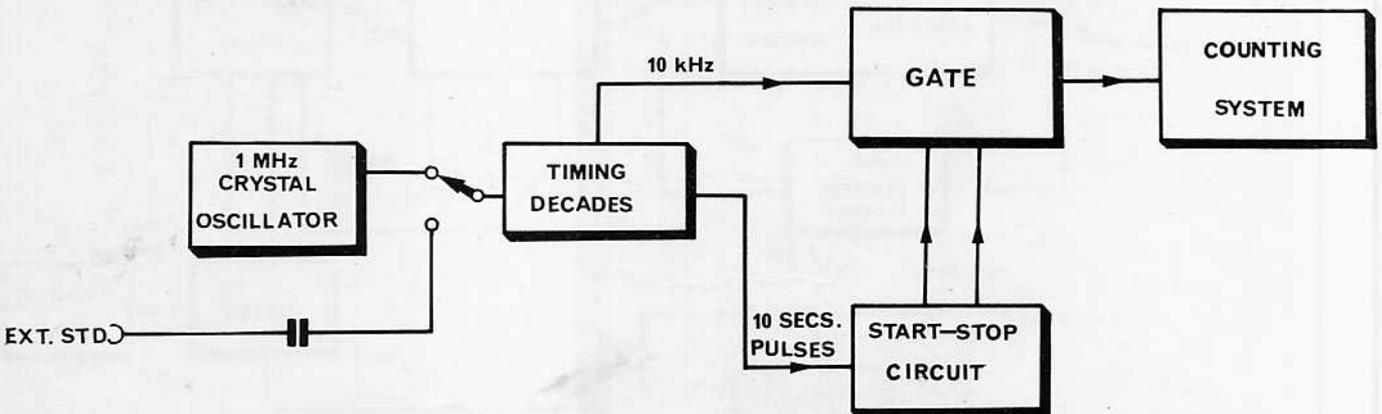


Fig. 6 Self-checking Facility

4.1 GENERAL

The instrument is composed of two main sections, the counter and the timing generator. The counter consists of an input circuit, an electronic gate and four decade counting circuits. The timing generator consists of a 1MHz crystal oscillator followed by a pulse shaping circuit, into which the external standard can be fed, and six divider stages.

When the instrument is used as a counter, incoming signals are amplified, converted into pulses of suitable shape and passed to the electronic gate. This gate is opened and closed by pulses from a start stop circuit and the signal pulses which are allowed to pass are registered on the counter.

The gate can be operated by:

- (a) Signals fed to the START-STOP sockets.
- (b) Signals generated by operating the START and STOP buttons.
- (c) Signals obtained from the crystal controlled timing generator.

In (a) or (b) the time intervals can be arbitrary, but in (c) the intervals for which the gate is opened are 0.001, 0.01, 0.1, 1 or 10 seconds. In condition (c) the instrument can be used for frequency measurement, the display indicating the frequency in kHz with an automatically positioned decimal point.

For period measurement the gate is opened by an incoming waveform via the input amplifier and the pulses from the timing generator are registered on the counter, thus indicating the period of the input waveform. The time interval between a pulse applied to the START socket and a pulse applied to the STOP socket can be indicated in a similar manner.

Full details of the arrangement of the individual circuits for each mode of operation are given in Section 3.

4.2 INPUT CIRCUIT (Fig. 8)

Under normal conditions the incoming waveform is amplified by the amplifier comprising VT1 to VT4 and applied to the trigger circuit comprising VT5 to VT7. The input circuit of the amplifier consists of VT1 and VT2 connected as a 'Darlington pair'. This circuit provides a high input impedance and high current gain, the voltage gain being close to unity. The transistors are protected from damage due to excessive input voltages by the diodes MT1 and MR2. The two amplifying stages VT3 and VT4 are of conventional design. To maintain the response at the lower frequencies large electrolytic coupling capacitors are used. Since the comparatively high series inductance of these capacitors would degrade the response at high frequencies, they are shunted by smaller capacitors of low inductance.

The trigger circuit is of a bistable type, and converts the input waveform into a square wave. To ensure fast rise and fall times, the emitter follower VT6 is employed for the coupling from VT5 collector to VT7 base.

For operation at very low frequencies (below approximately 10Hz) the input is taken directly to the trigger circuit comprising VT8 and VT9, by-passing the a.c. coupled amplifier. This trigger circuit is similar to that used for normal operation, except that the emitter follower coupling is not required at the lower frequency at which it operates. The diodes MR3 and

MR4 protect the circuit from damage due to excessive input voltages.

4.3 LOGIC CIRCUIT (Fig. 9)

(a) Start-Stop Circuit

The Start-Stop circuit consists of the three bistable circuits VT1/VT2, VT3/VT4, and VT5/VT6. Initially, after the counter has been reset, VT1, VT3 and VT5 are conducting. The positive going input pulses are applied via terminal 4 and C2 to the base of VT5. The first positive going edge cuts off VT5 and VT6 conducts.

Except when external start/stop pulses are being used, terminal 5 is connected via the switching circuits to terminal 6. Thus the positive going edge occurring at VT6 collector is fed via C1 to the base of VT1. This cuts off VT1 and VT2 conducts. The resultant positive going 'start' pulse at the collector VT2 is fed to the gate bistable, VT7 and VT8.

The second positive going input pulse cuts off VT6. The positive going edge occurring at VT5 collector is fed via terminal 7, the switching circuits, terminal 8 and C2 to the base of VT3. This cuts off VT3 and VT4 conducts. The resultant positive going 'stop' pulse at the collector of VT4 is fed to the gate bistable, VT7 and VT8.

External start and stop pulses may be fed directly to terminals 6 and 8. These pulses then trigger the bistables VT1/VT2 and VT3/VT4 in the same way as the pulses derived from the bistable VT5/VT6.

The negative going edge occurring at VT3 collector at the time of the 'stop' pulse is fed via terminal 11 to the display timer to initiate the display period.

(b) Gate Circuit

The pulses to be counted are applied to the bistable trigger circuit, VT11 and VT12. Transistors VT7 and VT8 form a bistable circuit with VT7 initially conducting. VT9 and VT10 form a parallel gate with VT9 held on by the negative supply via R20 since VT8 is cut off. The first 'start' pulse causes VT7 to cut off and VT8 cuts on and VT9 will now cut off.

If, due to a signal from the trigger circuit VT11 and VT12, VT10 is made to conduct, the gate output point will move from -10V towards earth thereby giving positive going pulses at the gate output. The gate output is applied to the input of the HF decade for all functions.

The 'stop' pulse causes VT8 to cut off and VT7 to conduct, VT9 then conducts and the gate output remains close to 0 volts, irrespective of the condition of VT10. Thus the input pulses are not transmitted through the gate.

The bistable VT7/VT8 is used for manual start-stop. The START and STOP push buttons are connected to terminal S9. For 'start' S9 is connected momentarily to the negative line and for 'stop' S9 is connected momentarily to earth.

The gate output point at the rear of the mother board can also be used for external gating. A low-impedance path to earth or a positive voltage can be used to clamp the gate shut. Alternatively, a positive pulse applied to this point would shut the gate for the duration of the pulse.

(c) Display Timer Circuit

The display time circuit is operated by the leading

edge of the negative-going pulse produced at the collector of VT3 in the stop circuit. This pulse is coupled via terminal 11, the AUTO/MANUAL switch. C19 and MR9 to the base of VT14. The diode MR9 holds back the positive-going trailing edge of the pulse.

The transistors VT14, VT15 and VT16 form a monostable circuit, VT14 being normally cut off and VT16 normally conducting. The negative going input pulse brings VT14 into conduction and the resulting positive-going step at the collector is applied via C20 and the emitter follower VT15 to the base of VT16. VT16 is then cut off, producing a negative-going step at the collector. This point remains negative until the charge on C20 has leaked away via R50 and RV1 sufficiently for VT16 to conduct. At this point the circuit reverts rapidly to its original condition. The emitter follower VT15 is used to prevent the comparatively low impedance at VT16 base affecting the discharge of C20.

The DISPLAY TIME potentiometer, RV1, allows the duration of the negative pulse at VT16 collector to be varied between 0.3 and 7 seconds. After reset the capacitor C20 recharges through R47 and the base-emitter diodes of VT15 and VT16. Since the time constant of C20 and R47 is approximately 12ms, events occurring in less than 12ms do not allow C20 to fully recharge and thus result in a shorter display time for any given setting of RV1.

The transistor VT17 is normally held conducting by R53. Since the pulse from VT16 collector is a.c. coupled to VT17 base via C21, the positive going (i.e. trailing) edge of this pulse cuts off VT17.

The resultant negative-going edge at VT17 collector is directly coupled to VT18 and VT19. These two transistors, one an *n-p-n* type and the other a *p-n-p* type, are both connected as emitter followers and provide a high current gain. Thus a reset pulse is produced.

For satisfactory operation of the bistable circuits, the reset line must reset at a stable potential of approximately +2 volts. This is achieved by the potential divider R54, R55. The reset pulse extends to very nearly -11 volts.

With the AUTO/MANUAL switch set to MANUAL, the monostable circuit VT14, VT15 and VT16 does not operate. The counter can then be reset manually by a positive pulse applied via C22 to VT17 base. This pulse may be derived either from the RESET push-button or externally.

The RESET push-button is fixed with a resistance/capacitance network to produce a pulse of fixed duration, thus preventing erratic resetting of the counter. The capacitor receives a charge from the positive line and is discharged, producing the reset pulse, when the RESET push-button is depressed.

For external reset, the requirements are a positive pulse of greater than 5 volts amplitude and having a duration of more than 20 μ s to ensure that VT17 is cut off. The pulse amplitude should not be greater than 15 volts, otherwise damage to VT17 may result.

4.4 DECADE COUNTER AND INDICATOR CIRCUIT (Fig. 10)

Due to the different maximum switching speeds of the four decade ring counters used in the instrument, the circuits differ slightly. The low-frequency counter

is described in detail below and the differences occurring in the medium-frequency and high-frequency counters are then enumerated.

The counter consists of a five-stage closed shift register, with inversion at one point in the ring. At the start of the count all five bistable stages are in the 'off' condition, i.e. even numbered transistors conducting. The first five input pulses will switch on each one in turn down the chain until all are on. The next five input pulses switch the bistables off in turn until at the tenth pulse the counter is reset to the original condition, thus providing a ten-cycle or decade counter.

The five bistable circuits VT1 to VT10 are identical and the positive-going input pulses are applied to both sides of all bistables. However, a bistable is only switched by an input pulse if it is primed by the preceding stage.

At the start of the count, when bistables are off, VT2, VT4 etc. will be conducting. Consider the bistable VT3 and VT4; its priming resistor, R18, is connected to VT1 collector, which is approximately -11 volts. Since the amplitude of the input pulse applied via C8 is approximately 8 to 10 volts, it does not raise MR4 anode sufficiently positive to cause the diode to conduct. Thus the bistable is not switched by the input pulse. The input pulse applied via C5 to VT3 base has no effect since the transistor is already cut off. Similarly the bistables VT5/VT6, VT7/VT8 and VT9/VT10 will not be switched.

However, the priming resistor, R9, of the bistable VT1/VT2 is connected to the collector of VT10 which, since VT10 is bottomed at approximately 0 volts. The input pulse therefore raises MR2 anode to approximately +8 volts, causing the diode to conduct and switching off VT2. The coupling then switches on VT1.

Now consider the effect of the next input pulse on the bistable VT3/VT4. Since VT1 is now bottomed, its collector is close to 0 volts. As the priming resistor, R18, is connected to VT1 collector, this input pulse raises MR4 anode to approximately +8 volts, causing the diode to conduct and switching the bistable. When VT3 conducts the bistable VT5/VT6 is primed in a similar manner so that it is switched by the next input pulse. This action continues down the chain until at the fifth pulse all bistables are on, i.e. the odd numbered transistors are bottomed and the even numbered transistors are cut off.

The collector of VT9 is connected to the priming resistor, R1, associated with VT1. When VT9 becomes bottomed at the fifth pulse, its collector rises to approximately 0 volts. This permits the next input pulse to cause MR1 to conduct, switching VT1 off and VT2 on. This in turn allows the next input pulse to switch off VT3/VT4 and so on down the chain until at the tenth pulse all bistables are returned to the off condition. The table inset on Fig. 4 shows the condition of all bistables for each of the ten digits 0 to 9.

All bistables may be returned to the off condition by a negative voltage applied to the reset line. This reset voltage is applied to the bases of all even numbered transistors to cause them to conduct.

The condition of the bistables is translated by transistors VT11 to VT20 to provide a one-of-ten-line drive for the indicator. The transistors VT11 to VT20 have

their bases and emitters coupled to the appropriate collectors of the bistables. As an example consider the digit '18'. This corresponds to bistable VT1/VT2 being switched on and all other bistables switched off. The '1' drive to the indicator is provided by VT12 which has its base connected to VT4 collector and its emitter to VT2 collector. For the digit '1' VT4 is bottomed (collector at 0 volts) and VT2 is cut off (collector at -11 volts), which are the conditions for VT12 to conduct. An examination of the table inset on Fig. 10 will show that this is the only combination of bistable conditions for which VT12 conducts. The drives for the other digits are derived in a similar manner.

On medium and high-speed decades the priming resistor have diodes (MR11 to MR20) connected in parallel to speed up the operation. Apart from this the circuit configuration is the same for all decades but component values and transistor types for the high speed decade differ from those for the low and medium-speed decades.

It should be noted that resistor R66 shown on Fig. 10 is replaced by a link, the actual resistor being fitted on the mother board in the power supply circuit.

Transistors VT21/VT22 form a push-pull emitter follower to buffer the input.

The neon NV1 lights to indicate the position of the decimal point. It is energized by the switch controlling the timing pulse generator to correctly position the decimal point.

4.5 TRIPLE DECADE CIRCUITS (Fig. 11)

Each triple decade board consists of three divide by ten circuits and, therefore, the circuit diagram has three references for each component. The diodes MR28 to MR34 inclusive are for speed-up purposes and are fitted to the first decade only, since in one position this decade operates at 1MHz. Two triple decade boards and one single decade board are fitted in the instrument, giving a total division of ten million.

Division by ten is achieved in two stages. The circuit first divides by two and then by five, hence it is said to be 'bi-quinary' counting. Division by two is carried out by VT1 and VT2, which form a conventional diode-steered binary with reset. Division by five is carried out by the three binaries VT3/VT4, VT5/VT6 and VT7/VT8, the hold diode MR7 converting the basic scale of six to a scale of five. The divide by five circuit functions as follows:

Initially, following reset, VT3, VT5 and VT7 are bottomed and VT4, VT6 and VT8 are cut off. The priming resistor R78 associated with VT5 is connected to VT7 collector, which is close to 0 volts. Thus the binary VT5/VT6 is triggered by the first input pulse. The priming resistors of VT3 and VT7 are connected to collector which, at this time, are at -11 volts. Thus the binaries VT3/VT4 and VT7/VT8 are not triggered by the first input pulse.

By similar process, only the binary VT3/VT4 is triggered by the next input pulse. At the third input pulse, the binary VT7/VT8 is triggered. At the same time binary VT5/VT6 is triggered back to its original condition, this being ensured by the hold-off diode MR7 which, when VT8 collector rises to 0 volts, pulls VT5 collector to 0 volts. At the fourth pulse the binary VT3/VT4 reverts to its original condition and finally at the fifth pulse the binary VT7/VT8 is

triggered, all binaries now being restored to their initial conditions.

The output is taken from the collector of VT6. A positive edge is produced every time VT6 is switched on, this being once every divide-by five cycle.

NOTE Diodes MR28 to MR35 are incorporated only in the first decade (VT1 to VT8) since this has to work at 1MHz in the timing generator.

4.6 SINGLE DECADE CIRCUIT (Fig. 11)

The description of this circuit is exactly the same as one of the triple decade circuits described in paragraph 4.5

4.7 1 MHz OSCILLATOR (Fig. 12)

Crystal XL1, VT4 and VT6 form the oscillator circuit, positive feedback being applied between the emitter of VT6 and the emitter of VT4. At any other frequency than 1MHz the crystal forms a very low impedance. The attenuation is lowest and the gain highest at the series resonant frequency and this determines the frequency of oscillation within the oscillator loop. There is, however, a phase shift, due mainly to variation in transistor parameters, and this is corrected by the three parallel capacitors C8, C5 and C7 which are in series with XL1. C8 is selected for its stable temperature co-efficient and has a nominal value. C5 is a coarse trimmer the value of which is variable between 4 and 60pF, and is mounted beside the crystal oven on the mother board. C7 is a fine trimmer which is variable between 1.5 and 8pF and is mounted under the crystal oven on the mother board. The tuning screw of C7 is accessible through the grill on the right-hand side unit panel.

VT5 is an emitter follower which presents only a very light load to the oscillator section and acts as a buffer to the pulse shaper stage, VT7 and VT8. The output of VT5 is connected via C11, a closed link on the EXT. STANDARD socket and C12, to the base of VT7. The pulse shaper stage, VT7 and VT8 changes the shape of the 1MHz oscillation from VT5 so that it becomes the rectangular form required to operate the decades. If a plug is placed into the EXT. STANDARD socket, the output from VT5 is disconnected from VT7 base and a variety of suitable waveshapes and pulses can be applied from an external source to VT7 to provide a 'standard' frequency. The pulse shaper stage is supplied directly from the -11V line but the oscillator is supplied with a stabilized -7V which is obtained from the -11V line via MR4 and R7 in the power supply circuit.

4.8 POWER SUPPLIES (Fig. 13)

The power supplies consist of a conventional series/parallel supply transformer T1, with three secondary windings which supply the following voltages:

- 215V. This voltage is rectified by the selenium bridge rectifier MR6 and, after smoothing, supplies the h.t. to the neon digit and decimal point indicators.
- 18V. This voltage is rectified by the bridge rectifier MR5 and smoothed. An emitter follower VT2, referenced to the Zener diode MR3 stabilises the output line at -11 volts. A -7 volts supply for the 1MHz Oscillator is derived from the -11 volts line by the Zener diode MR4 and R7. In addition series resistor R27 is included to provide a -10V supply to the input shaper.

- (c) 12V. The 12V winding of T1 supplies the heater of the crystal oven. In addition a half wave rectifier consisting of MR1, r.c. smoothing, Zener diode MR2 and emitter follower VT3 provides a stabilised +8V supply.

NOTE The stabilised voltages stated above are nominal, in practice the measured voltage may be very slightly above or below the stated figure due to component tolerances.

4.9 PRINTER ADAPTOR CIRCUIT (Fig. 14)

The printer requires an initiate pulse to start the printing cycle. This is derived from the stop pulse in the counter which occurs when the counter gate is closed. The positive going edge from the counter is applied to the base of VT8 via R18 and C8, which differentiate the edge to form a pulse, and the output from the collector of VT8 is taken to the printer.

It is necessary to prevent the counter from starting another measurement until the printer has finished interrogating the decades. The stop signal which starts the display timer is taken to the display timer via a diode gate, MR12, R19. If the printer is not connected to the counter the signal passes to the display timer in the usual way, but when the printer is connected contact NK¹ in the printer earths the junction of MR12 and R19, so preventing the stop signal from reaching the display timer. The operation of the stop bistable is not affected since MR12 is reverse biased by the signal from the stop bistable. After the printer has provided ten pulses the interrogation is complete and contact NK¹ opens, allowing the junction of MR1 and R19 to go negative, which starts the display timer.

The counter decades are normally connected in cascade, but must be isolated from each other whilst the printer interrogates them, so that they can be driven simultaneously in parallel. This is done by the diode gates MR2, MR3 and MR4, MR5, etc., under the control of printer contact NK₂. This contact is normally open so that VT1 conducts and the junction of R2 and C1 is held at a negative voltage. R2 and C1 ensure that any voltage changes are slow ones which

will not cause an unwanted step of the decades when NK₂¹ operates.

The negative voltage at R2, C1 junction is applied to R3 to R7 and also through R8 to the pulse input line which is capacitively coupled via C2. The 'carry' output from one decade to the next operates between 0V and -11V, and so can pass through MR2, MR4, etc., to the next decade, the diodes always being forward biased or having zero voltage across them. Diodes MR3, MR5, etc., are always reverse biased.

When contact NK₂¹ closes during printing, VT1 is cut off and C1 discharges to 0V via R2, MR1, and MR13, so connecting 0V to resistors R3 to R8. (MR1 is necessary to by-pass the cut-off transistor VT1, and MR13 is necessary when two counters are connected to a common printer to prevent current flow between the two negative supplies). MR3, MR5, etc., will conduct positive going signals to the decade inputs. Note that the decade inputs are a.c. coupled, and that during normal operation the decade input voltage swing is between -11V and 0V, whilst during print-out it is between 0V and +11V due to differentiation of the stepping pulses in C2.

The stepping pulses are generated by a slotted disc, lamp, and photocell in the printer and are squared-off by VT4. The push-pull emitter follower VT2, VT3 provides a low source impedance to drive all the decades in parallel.

The first decade in the counter has to be capable of working up to 5MHz, or 10MHz in the case of TC6, and a diode gate will not operate satisfactorily at this speed. The gating for the first decade is done by a parallel transistor gate VT6, VT7. During normal counting VT4 is cut off, VT5 conducts, and so VT6 is non-conducting. The signal from the counter main gate output therefore operates VT7 and passes to the input of the first decade. At the end of the measurement the counter gate closes and applies 0V to VT7 base, making it non-conducting. The printer stepping pulses now operate VT6 via VT4 and VT5, and step the first decade.

The 'carry' pulses are taken to lock the appropriate print wheels via differentiating circuits and buffer amplifiers VT9 to VT14.

5.1 REMOVAL OF CASE

Access to internal components is obtained by removing the four screws at the rear of the case, and then pulling the case clear of the instrument.

5.2 FUSE REPLACEMENT

The instrument is protected against accidental internal short circuits by three fuses, F1 in the a.c. supply, F2 in the -11V line and F3 in the +8V line. These fuses are mounted on the small panel at the rear of the mother board and are accessible from the rear of the instrument when the case has been removed. F2 and F3 are on the panel beside the alternative voltage switch and F1 is behind the panel. (See Fig. 16).

NOTE When the printer adaptor board is fitted the supply fuse F1 is below F2 and F3, so that it will be accessible after the board is fitted.

WARNING The supply fuse is now exposed, therefore extra care must be taken when the case is removed.

Only fuses of the same type, rating and value should be used and these are clearly stated in Section 6.8, page 24.

5.3 OSCILLATOR FREQUENCY ADJUSTMENT

When the equipment is despatched from the factory, the oscillator will have been set for the greatest accuracy in the ambient temperature range +20°C to +25°C. In keeping with a characteristic of all crystal oscillators, ageing takes place over a period of time, resulting in a slight drift of frequency. The amount of drift is not predictable and, if the best performance is desired, it is advisable to check against a standard frequency, say every three months and to correct where necessary.

It is necessary to have access to either a frequency standard whose accuracy is equal to or better than 1 part in 10 million or a straight receiver tuned to the 200kHz Light Programme transmission from Droitwich. Modulation on the latter is likely to cause difficulties so that it will be necessary either to wait for programme breaks or to devise a method for removing the modulation.

By using the Advance Off-Air Frequency Standard OFSI, modulation problems are overcome. For further details, send to Advance Electronics Ltd.

The standard frequency and the 1MHz output of the counter should be displayed on an oscilloscope to form a Lissajous figure. This should produce a stationary figure with five traverses of the counter frequency for one traverse of the Droitwich signal. Use the trimmer capacitors C5 (coarse) and C7 (fine), adjacent to the crystal oven, to adjust the counter frequency. Allowances should be made for the warming-up time of the crystal oven and cycling of the crystal as the oven is automatically switched on and off, refer to paragraph 3. 2(e). Alternative use the Advance Off-Air Frequency Standard OFSI.

5.4 OPERATIONAL CHECK

A check on the correct functioning of the counter may be carried out as follows:

- (a) Check that the external standard (EXTERNAL STANDARD) jack plug has been removed.
- (b) Remove the instrument from its case (paragraph 5.1).
- (c) Check that the voltage switch is correctly positioned for the supply used.

- (d) Set the function switch to the CHECK position.
- (e) Switch on the supply and press the RESET button. The instrument should count 10kHz pulses for 1 second then indicate 0000 ± 1 count.

If the instrument fails to perform the above function, set the function switch to TIME and press the RESET button. The instrument should indicate 0000 ± 1 .

If the instrument fails to do this the power supply output voltages should be checked having first read paragraph 4.8. These should be as follows:

-11V, +8V, +2V bias. The 'reset' line should rest at +2V.

If a circuit failure should occur it is advisable to return the counter to the manufacturer for investigation whenever this is possible. When this is not possible refer to paragraph 5.5.

5.5 GUIDE TO SERVICING

The servicing of the TC4A counter is simplified by the fact that most of the boards are interchangeable. Faults can therefore be rapidly traced, in many cases, to a particular board by substitution tests. A brief outline of a test sequence is given below.

NOTE It is assumed that before these tests are started, the procedure given in 5.4 has been carried out.

Any ring counter is faulty which fails to indicate 0 when reset as in paragraph 5.4 and when all voltages are correct. Alternatively the mother board connections are in some way faulty. The suspect faulty board should then be transferred to any position which shows 0, even if it is an H.F. or M.F. board, since all ring counter boards will work in any position (the only difference between boards is the maximum frequency up to which they will operate).

If the counter displays 0000, set the UNIT TIME SECS. switch to 1. Press the START button, the right-hand indicator should proceed from 0 to 9 in 10 secs.

If it does not, check the following 1MHz outputs using an oscilloscope on the rear of the mother board.

- ES1 1MHz
- ES2 1MHz
- 1MHz O/P 1MHz

If 1MHz is not present at ES1 the fault is in the crystal oscillator.

If 1MHz is present at ES1 but not ES2 it is the external standard socket or wiring which is incorrect.

If 1MHz is present at ES2 but not at the 1MHz O/P, it is the 1MHz trigger circuit which is faulty.

If the 1MHz signals are present the triple decade outputs should be checked at the front panel OUTPUT P.P.S. socket to the table given below:

Setting of UNIT TIMES secs. switch	Output Frequency	Test Ref.
10 ⁻⁶	1MHz	A } 1st board
10 ⁻⁵	100kHz	
10 ⁻⁴	10kHz	
10 ⁻³	1kHz	
10 ⁻²	100Hz	D } 2nd Board
10 ⁻¹	10Hz	
1	1Hz	
10	0.1Hz	Single Decade

Table 5.1 Output P.P.S. for UNIT TIMES sec. switch positions

If one of these outputs is not seen, it is the decade following the highest frequency present which is either faulty, not connected or not driven correctly.

The two triple decade boards are identical so that normally a fault can be rapidly located by interchanging the boards. If, for example, the fault occurred on one of the tests A to C, interchanging the boards would move the fault to the corresponding test on D to F. Similarly, if one of the low frequency outputs was faulty, interchanging the boards would produce a fault on one or more of the outputs A to C.

If all the outputs are correct, but the right-hand indicator does not count, the fault must be on the logic board or functioning wiring. The most likely place is the gate circuit on the logic board.

If the right-hand indicator progresses from 0-10 in the appropriate time for all settings of the UNIT TIME SECS. switch, but the counter still fails to check, the fault is probably either in the Start/Stop circuit of the logic board or in the functional wiring.

If the counter checks but fails to measure frequency or periods, the fault is either in the input circuits, logic, or wiring.

The normal and V.L.F. trigger circuits are independent except for the positive line and wiring. Faults on these circuits can therefore be eliminated by means of the V.L.F./NORMAL switch (i.e. it is unlikely that both circuits will be faulty simultaneously).

NOTE The test signal should meet the V.L.F. input requirement for level and should be at a higher frequency than 10.

The pulse from the final trigger stage of the input circuit should be a square pulse of about 8V in amplitude moving from the negative line to 0V. If this is correct the fault will be possibly in the wiring or in the logic board (probably the gate or the gate trigger circuits).

If, on pushing the reset button, a pulse of about 12V connected to a reset line, the fault is in the display timer circuit or on the reset line itself.

It should be noted that providing the RESET push button and its associated wiring are functioning correctly switching to 'auto' will not help to diagnose the fault. In general the counter will only work in 'auto' if it works manually. If the counter works manually but not on auto the fault will probably be in the Display Timer circuit, VT14, VT15, VT16, or in the associated potentiometer RV1 and its wiring.

If the counter behaves correctly on all internal functions such as frequency and period measurement and appears to give trouble when used for external timing via START and STOP sockets it is recommended that a careful examination of the pulses applied at these sockets is carried out using a high performance oscilloscope:

- (a) To see that the pulses meet the input requirements for the START and STOP sockets.
- (b) To ensure that there is a clean pulse being fed to the sockets, particularly on single line working fed from inductive circuits or mechanical contacts.

5.6 WAVEFORMS (Fig. 7)

The following waveforms should be observed by using a high performance oscilloscope with a suitable probe attachment i.e. A Tektronix oscilloscope, type 541. The waveforms shown in Fig. 7, which are not idealized, are, as near as possible, an accurate representation of the traces obtainable from a counter which is functioning correctly under 'no input' conditions.

Waveform 1 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-6}

Oscilloscope timebase setting: 1 μ sec./cm.

Waveform 2 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-5}

Oscilloscope timebase setting 2 μ sec./cm.

Waveform 3 Taken from the OUTPUT P.P.S. socket.

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-4}

Oscilloscope timebase setting: 20 μ sec./cm.

Waveform 4 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-3}

Oscilloscope timebase setting: 200 μ sec./cm.

Waveform 5 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-2}

Oscilloscope timebase setting: 2ms/cm.

Waveform 6 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 10^{-1}

Oscilloscope timebase setting: 20ms/cm.

Waveform 7 Taken from the OUTPUT P.P.S. socket.

Counter control settings:

- (a) Count set to COUNT 2 LINE
- (b) UNIT TIME SECS. set to 1

Oscilloscope timebase setting: 100ms/cm.

Waveform 8 Taken from the OVERSPILL socket.

Counter control settings:

- (a) Count set to TIME 2 LINE
- (b) UNIT TIME SECS. set to 10^{-6}

Oscilloscope timebase setting: 200ms/cm.

NOTE The positive-going edges of waveforms 1 to 7 are the parts to be noted as these are time related. The edges of waveform 8 are not related to the other seven.

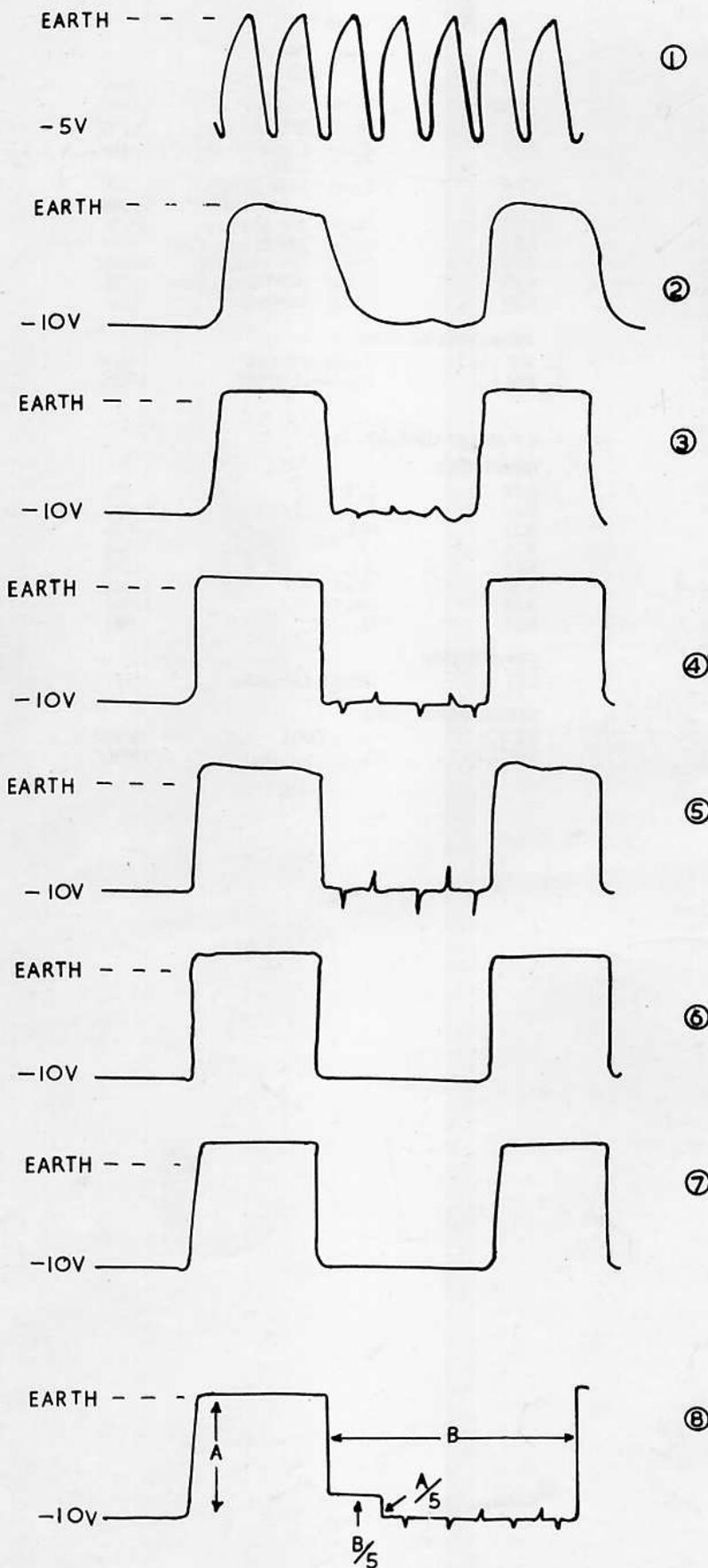


Fig. 7 Waveforms

6.1 INPUT CIRCUIT—NORMAL**RESISTORS (RRC type 5SWD18 5%, unless specified)**

Circuit Ref.	Value	Type	Part No.
R1	1K		384
R2	15K		315
R3	2.2K		425
R4	1K		384
R5	150Ω		301
R6	4.7K		386
R7	33K		317
R8	220		304
R9	1K		384
R10	150Ω		301
R11	4.7K		386
R12	1.8K		310
R13	1K		384
R14	1.5K		385
R15	1K		384
R16	820Ω		1637
R17	220Ω		304
R18	1M		766
R29	15K		315
R31	100K	10% ERIE 16	1270
R32	100		11504

CAPACITORS

C1	25μF	25V Mullard	20776
C2	2000pF	Lemcolac	1532
C3	1000pF	Lemcolac	1527
C4	25μF	25V Mullard	20776
C5	2000pF	Lemcolac	1532
C6	400μF	25V Mullard	20784
C7	1000pF	Lemcolac	1527
C8	15pF	Lemco 310N150	3002
		TE	
C10	0.1μF	400V WIMA	
		Trop. M	2385

Circuit Ref.	Value	Type	Part No.
C13	25μF	25V Mullard	20776
C14	22pF	Lemco 310N150	3310
		TE	
C15	0.1μF	125V WIMA	
		Trop. M	2740
C16	25μF	25V Mullard	20776
C17	0.05μF	30V Plessey Case	2793
C18	400μF	25V Mullard	20784
C19	0.05μF	30V Plessey Case	2793
C20	0.01μF	Lemcolac	4737

SEMICONDUCTORS

VT 1 to 7	Texas 2N711A	1634
MR 1, 2	Hughes HG1087	17956

6.2 INPUT CIRCUIT—VLF**RESISTORS**

R21	2.2K	425
R22	4.7K	386
R23	68K	1636
R24	1K	384
R25	22K	1544
R26	100Ω	11504
R27	10K	11503
R28	1K	384

CAPACITORS

C12	1000pF	Lemcolac	1527
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SEMICONDUCTORS

VT 8, 9	Texas D535	3610
MR 3, 4	Hughes HG1087	17956

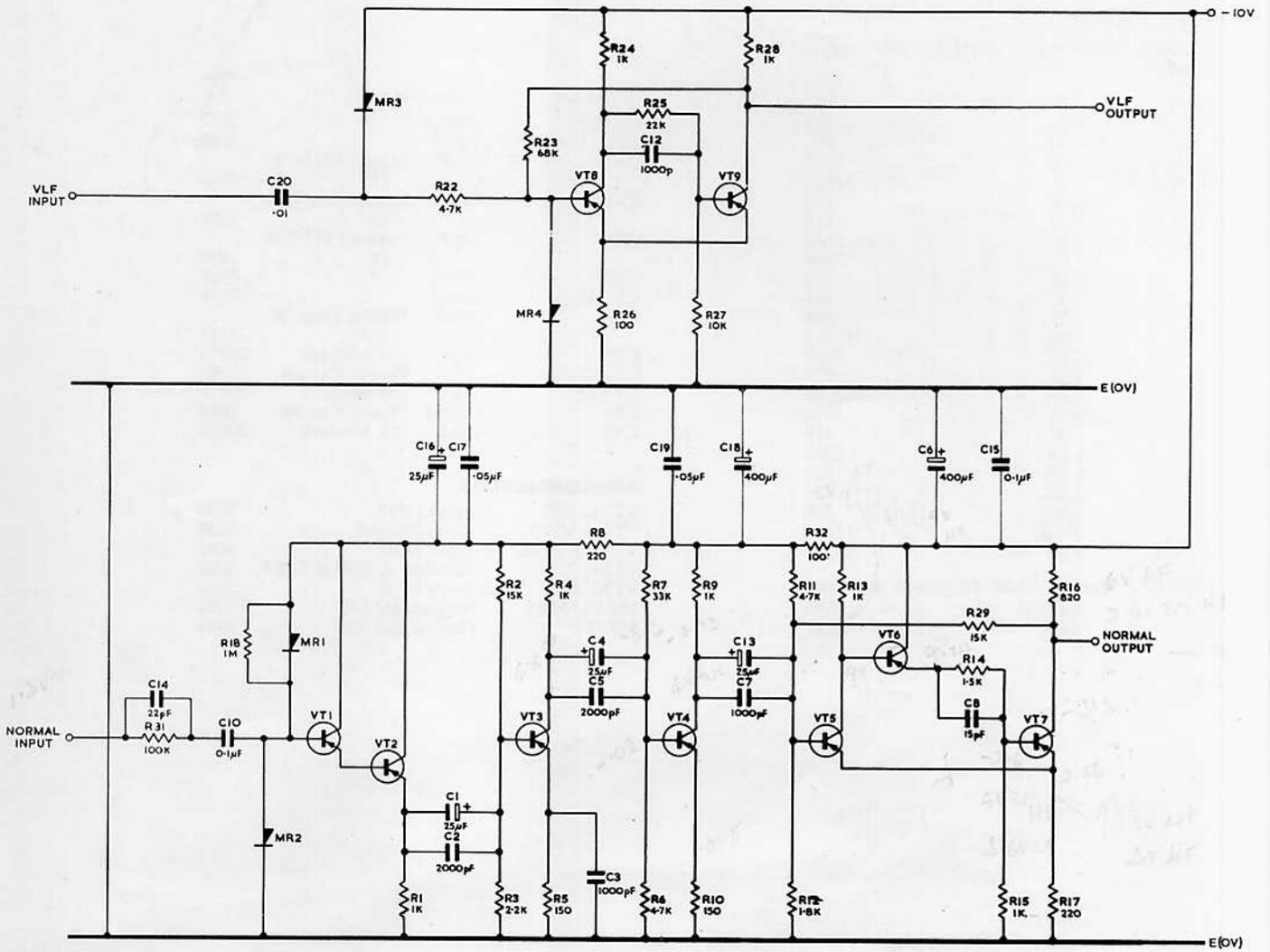


Fig. 8 Input Circuit—Normal and V.L.F.

6.3 LOGIC CIRCUIT

RESISTORS (RRC type 5SWD18 5%, unless specified)

Circuit Ref.	Value	Type	Part No.
R1 to R10	10K		11503
R11, R12	47K		318
R13 to R23	1.2K		2087
R25 to R33	10K		11503
R23, R35	6.8K		313
R36 to R39	47K		318
R41	22K		1544
R42	12K		1685
R43	6.8K		313
R44	15K		315
R45	4.7K		386
R46	10K		11503
R47	1.2K		2087
R48	47Ω		727
R49	1.2K		2087
R50	68K		1636
R51	15K		315
R52	1.2K		2087
R53	6.8K		313
R54	2.2K		425
R55	560Ω		308
R56	100Ω		11504
R57 to R60	10K		11503

CAPACITORS (Lemco 310K TE unless specified)

C1, 2	1000pF	2594
C3, 4, 5, 6	220pF	2588

Circuit Ref.	Value	Type	Part No.
C7, 8, 9	1000pF		2594
C10, 11, 12	220pF		2588
C13	33pF	Lemco 310 N150 TE	4768
C14	39pF	Lemco 310 N150 TE	4769
C15	10pF	Lemco 310 N150 TE	3000
C16	330pF		2590
C17, 18	220pF		2588
C19	.01μF	WIMA Trop. M 400V	3399
C20	20μF	25V Mullard	20775
C21, 22	.05μF	Plessey Cascap	2793
C23, 24	20μF	25V Mullard	20775
C29	0.02μF	Plessey Cascap	2663
C30	20μF	25V Mullard	20775

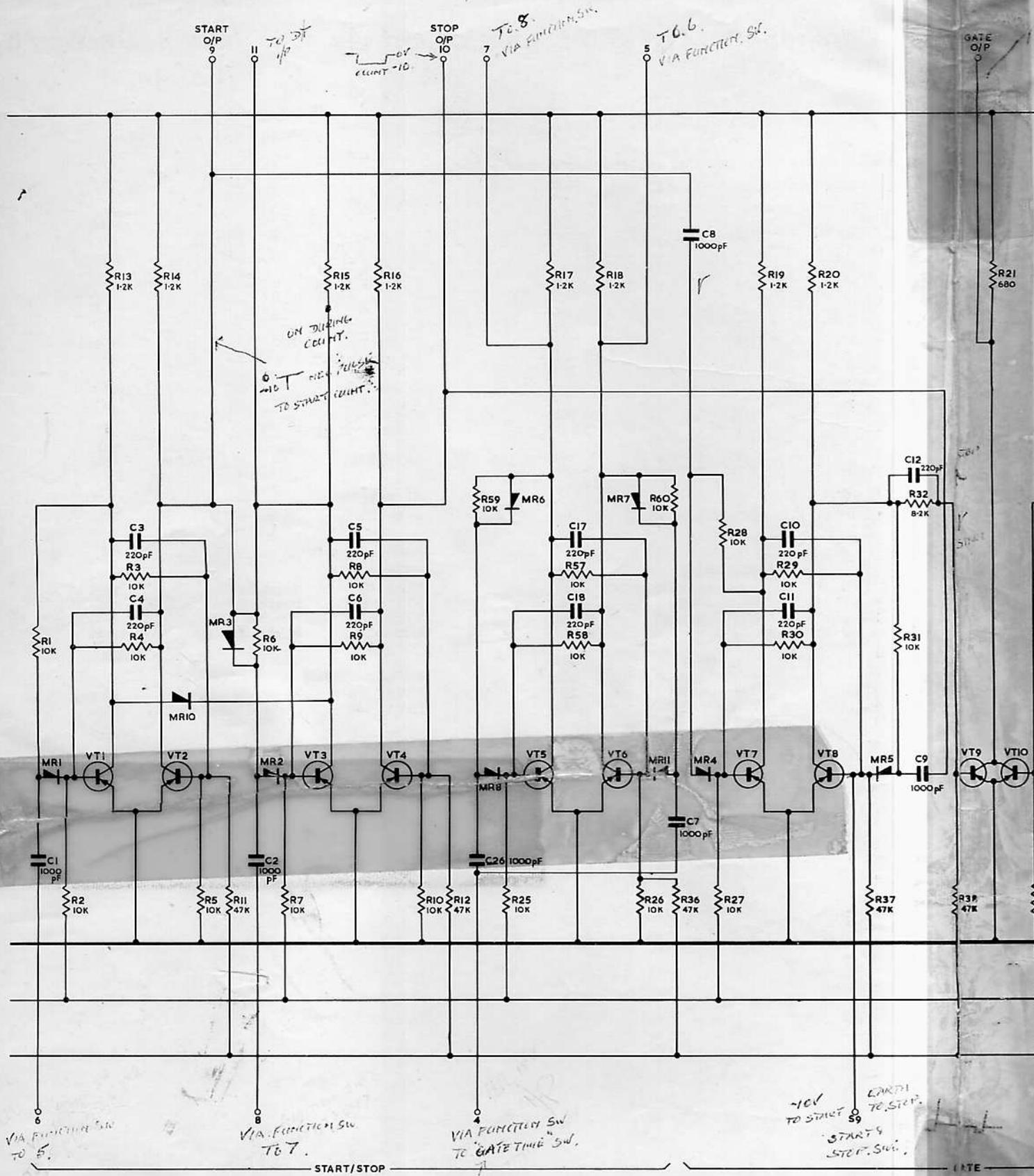
SEMICONDUCTORS

VT1 to VT8	Texas D535	3610
VT9 to VT12	Texas 2N711A	1634
VT14 to VT18	Texas D535	3601
VT19	Fairchild A 1670 or C407	4015
VT20, VT21, VT22	Texas D535	3610
MR1 to MR9	Hughes HG 1087	17956
MR11	Hughes HG 1087	17965

6. 10V REF. SOURCE VIA GATE DRIVE
 7. 10V REF. SOURCE VIA GATE DRIVE
 8. 10V REF. SOURCE VIA GATE DRIVE
 9. 10V REF. SOURCE VIA GATE DRIVE
 10. 10V REF. SOURCE VIA GATE DRIVE
 11. 10V REF. SOURCE VIA GATE DRIVE
 12. 10V REF. SOURCE VIA GATE DRIVE

Fig. 9 Logic Circuit





VIA FUNCTION SW TO 5.

VIA FUNCTION SW TO 7.

VIA FUNCTION SW TO GATE TIME SW.

-10V TO START STOP SW. EARTH TO STOP SW.

START/STOP

(NTE)

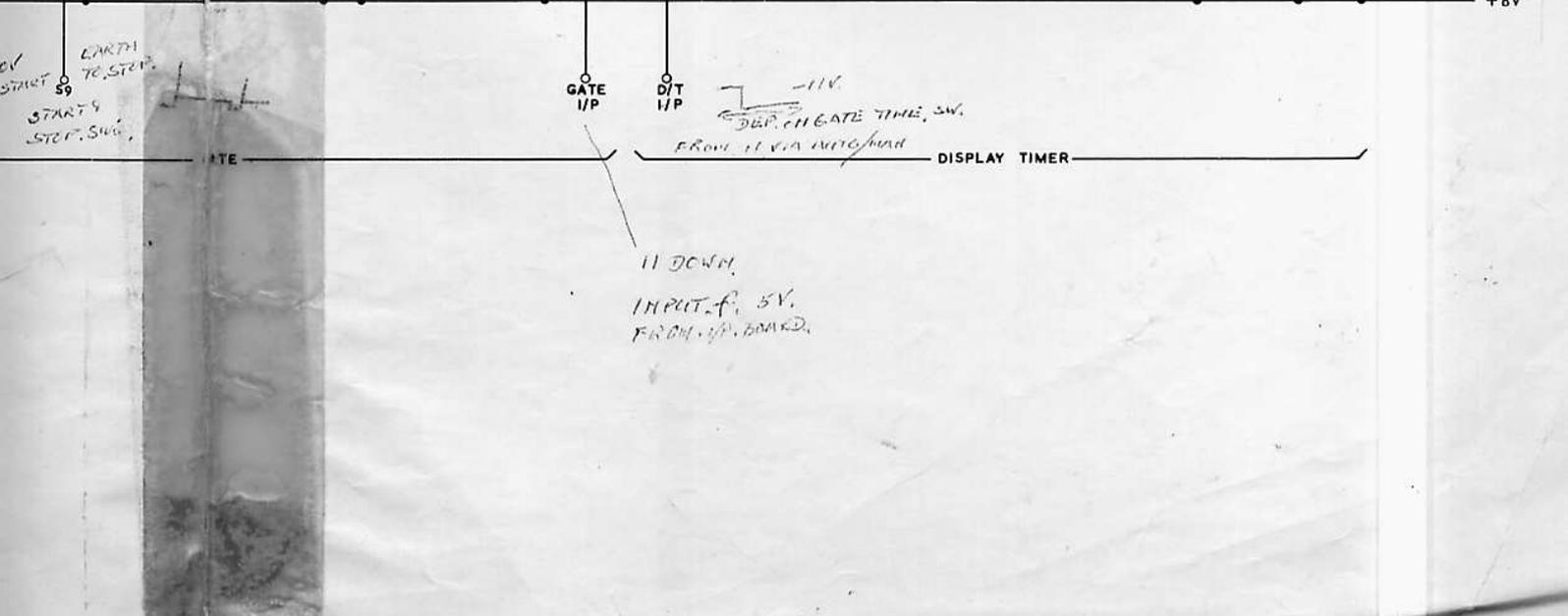
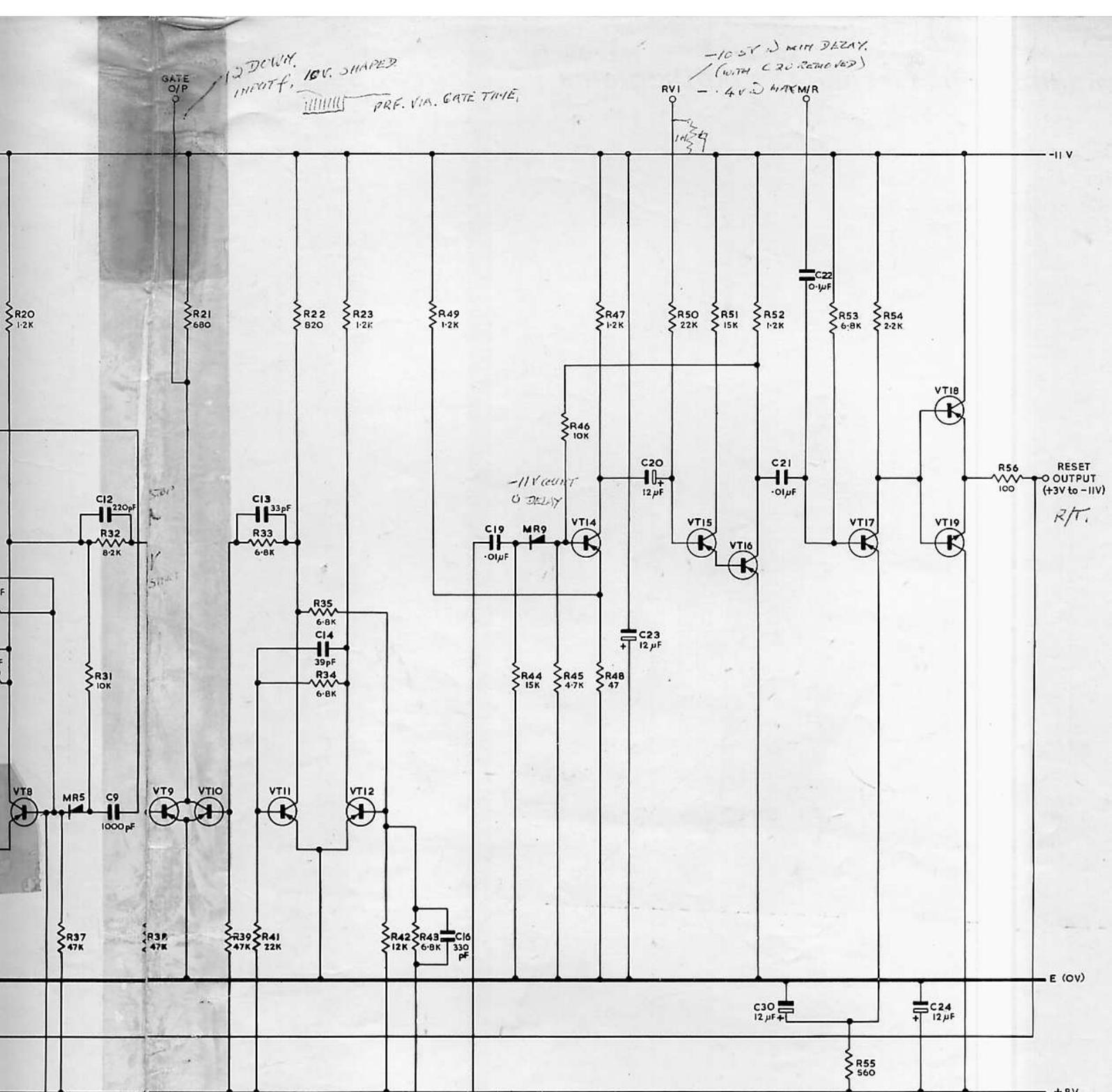
START OF SEQUENCE.

ON DURING COUNT.
TO START COUNT.

Tc 8 VIA FUNCTION SW.

Tc 6 VIA FUNCTION SW.

0V CLAMP -10



6.4 L.F., M.F., H.F. DECADE AND INDICATOR BOARDS

RESISTORS (RRC type 5SWD18 5%, unless specified)

L.F. and M.F. Boards

Circuit Ref.	Value	Type	Part No.
R1, 5, 6, 8, 9, 10, 14, 15, 17, 18, 19, 23, 24, 26, 27, 28, 32, 33, 35, 36, 37, 41, 42, 44, 45	10K		11503
R2, 11, 20, 29, 38	47K		318
R3, 12, 21, 30, 39	12K		1685
R4, 7, 13, 16, 22, 25, 31, 34, 40, 43	1.2K		2087
R46, 48, 50, 52, 54, 56, 58, 60, 62, 64	68K		1636
R47, 49, 51, 53, 55, 57, 59, 61, 63, 65	56K	1/2W Erie 16	3435
R67 to R76	3.3M	10% RRCLX	4016

CAPACITORS

C1 to C20	220pF	Lemco 310 k	2588
-----------	-------	-------------	------

SEMICONDUCTORS

LF Board only

VT1 to 10, 22	Texas D535	3610
VT11 to 20	Fairchild A1670 or C407	4015 <i>Part 17</i>
VT21	Texas 2N1302	3702
MR1 to 10	Hughes HG1087	17956

MF Board only

VT1 to 10, 22	Texas D535	3610
VT11 to 20	Fairchild A1670 or C407	4015
VT21	Texas 2N1304	2602
MR1 to 20	Hughes HG1087	17956

H.F. Board

Circuit Ref.	Value	Type	Part No.
R1, 5, 6, 9, 10, 14, 15, 18, 19, 23, 24, 27, 28, 32, 33, 36, 37, 41, 42, 45	5.6K		787
R2, 11, 20, 29, 38, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65	39K		1639
R3, 12, 21, 30, 39	12K		1685
R4, 7, 13, 16, 22, 25, 31, 34, 40, 43	470	5%	18546
R8, 17, 26, 35, 44	10K		11503
R46, 48, 50, 52, 54, 56, 58, 60, 62, 64	68K		1636
R67 to R76	3.3K	10% RRCLX	4016

CAPACITORS

C1 to C20	33pF	310 N150	4768 ✓
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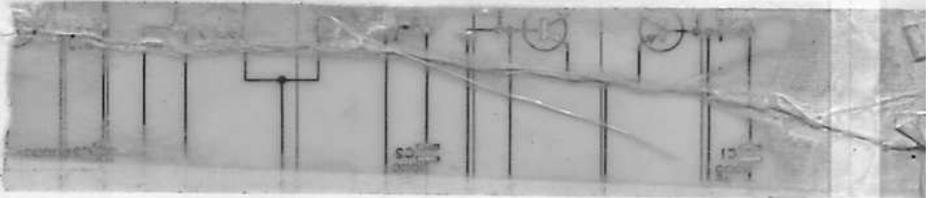
SEMICONDUCTORS

HF Board only

VT1 to 10	Texas 2N711A	1634 ✓
VT11 to 21	Fairchild A1670 or C407	4015 ✓
VT22	Fairchild V205	3307 ✓ <i>BSY 41</i>
MR1 to 20	Hughes HG1087	17956 ✓

MISCELLANEOUS

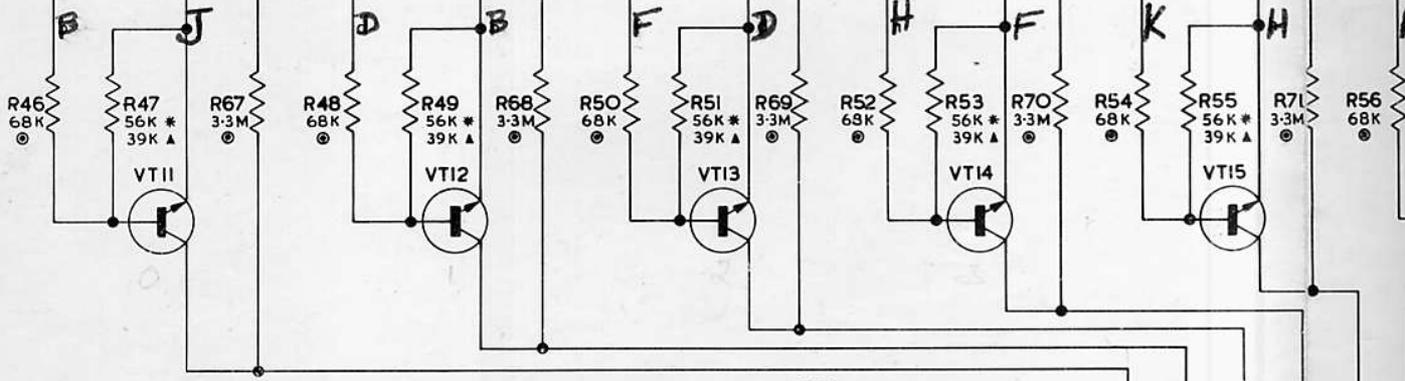
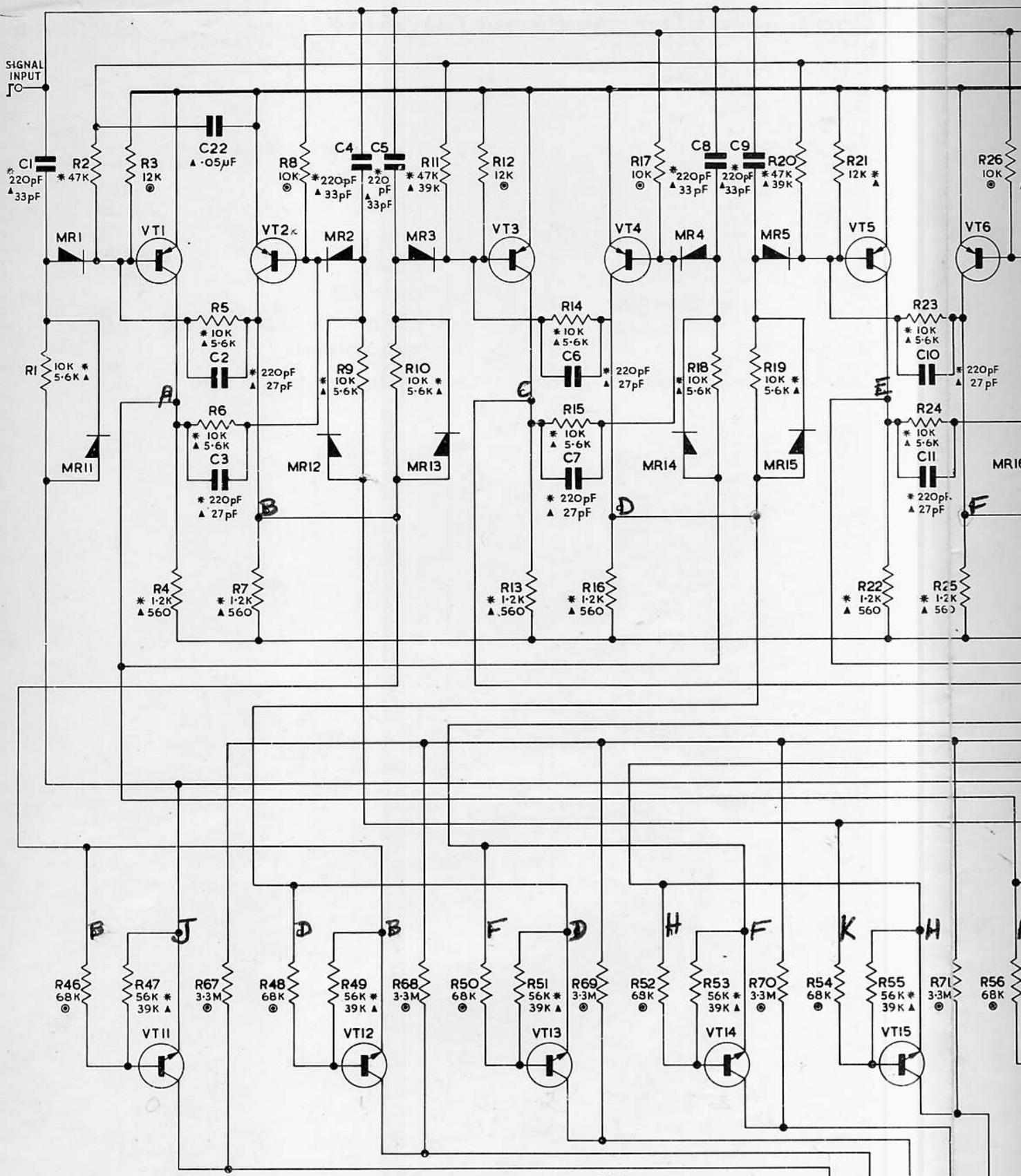
HIVAC XN.3	Numerical Indicator	4026 ✓
HIVAC 15L	Decimal Point Indicator	4916 ✓



Faint handwritten notes and markings on the page, including:
 B-J-20
 T-3-10K-100-2
 A-K-25
 K-9-100-20

Fig. 10 Decade Counter and Indicator Circuit

K C A M C M A C K
R M B C M A C K



x OFF
 • ON

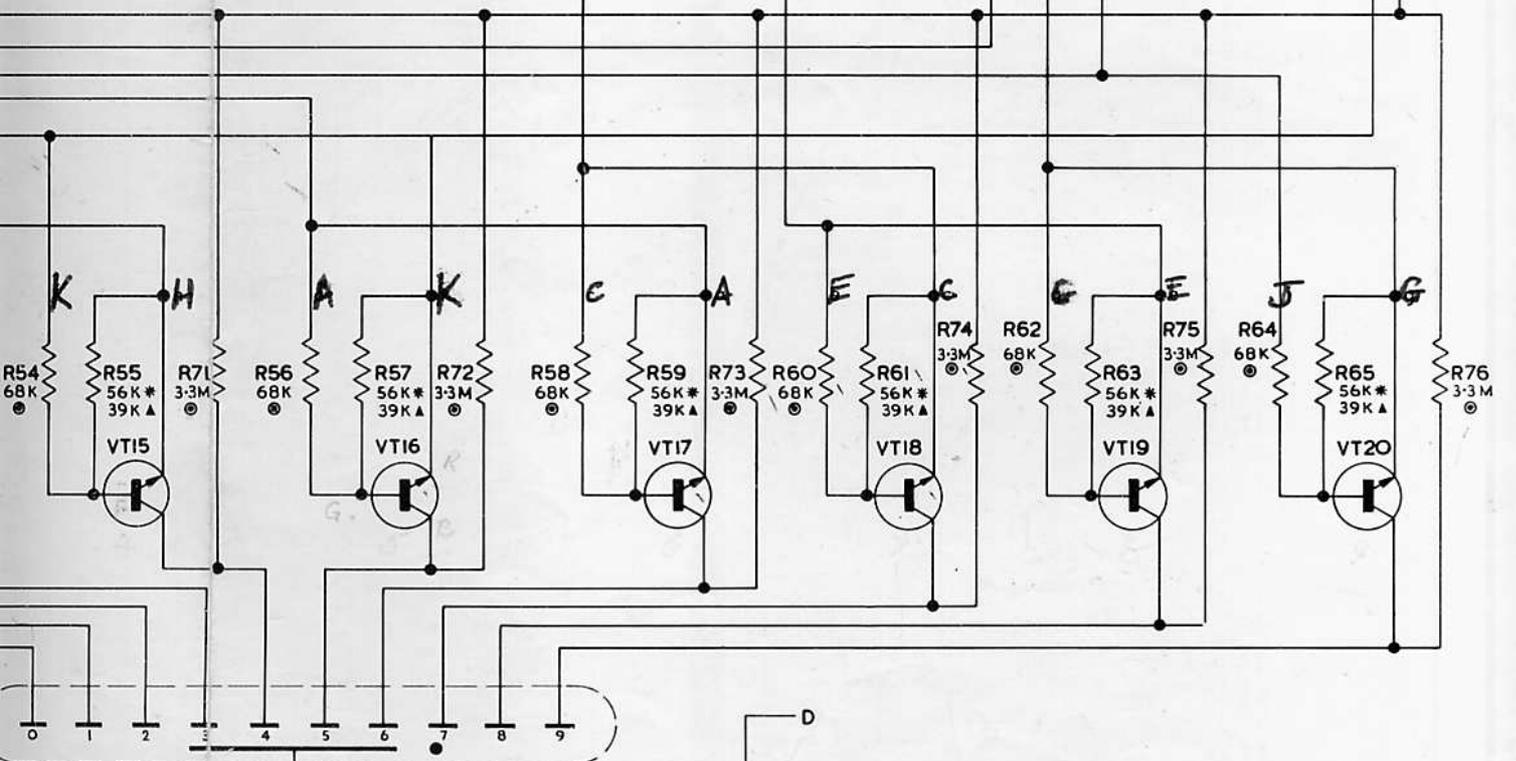
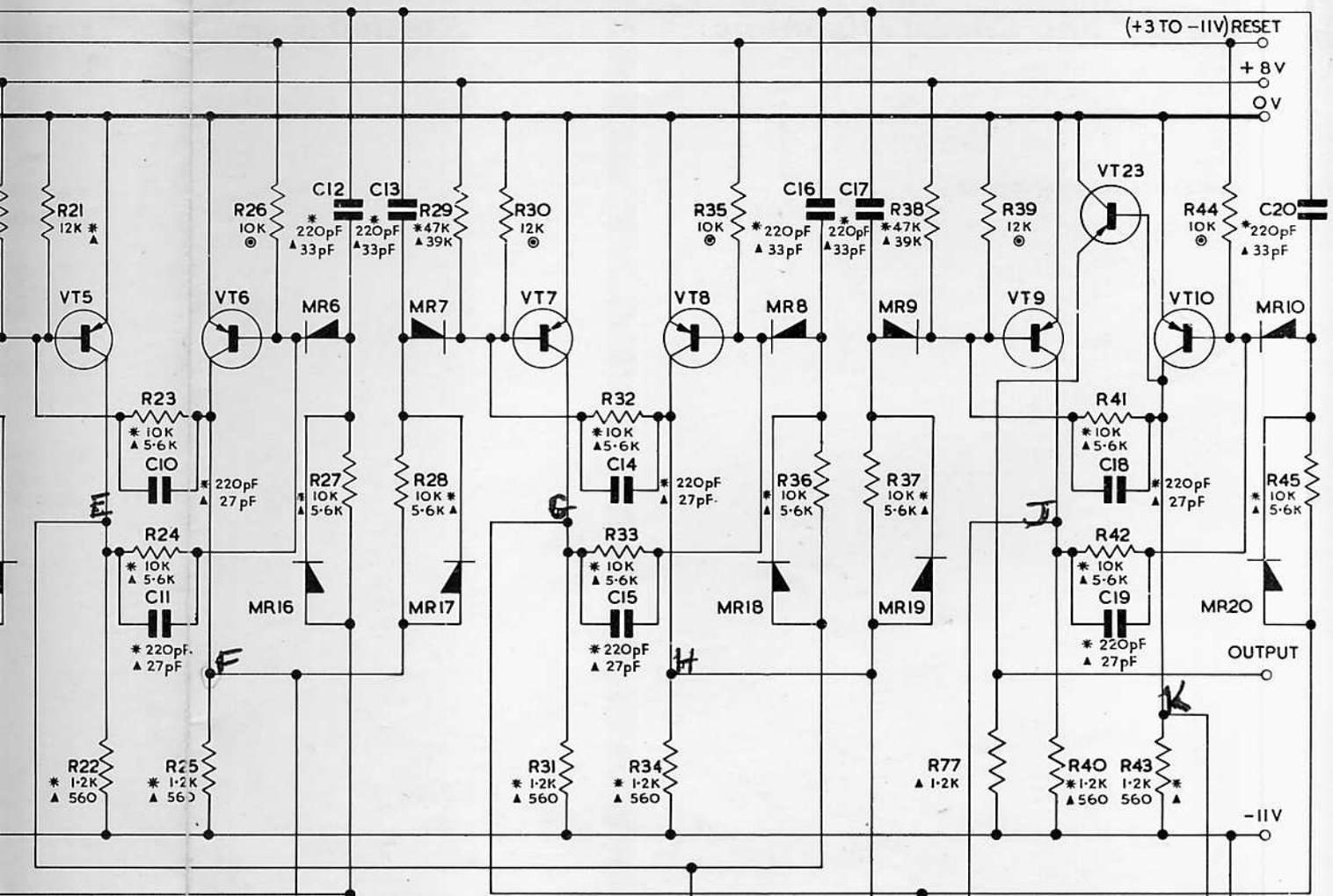
	a	b	c	d	e	f	g	h	j	k	
0	x	x	x	x	x	x	x	x	x	x	← RESET
1	x	x	x	x	x	x	x	x	x	x	
2	x	x	x	x	x	x	x	x	x	x	
3	x	x	x	x	x	x	x	x	x	x	
4	x	x	x	x	x	x	x	x	x	x	
5	x	x	x	x	x	x	x	x	x	x	
6	x	x	x	x	x	x	x	x	x	x	
7	x	x	x	x	x	x	x	x	x	x	
8	x	x	x	x	x	x	x	x	x	x	
9	x	x	x	x	x	x	x	x	x	x	

NOTES

1. R66 NOT USED.
2. MR11-MR20 NOT FITTED TO LF DECADES.
3. VT21 & VT22 NOT FITTED ON L.F. DECADES.

0
 1
 2
 3
 4
 5
 6
 7
 8
 9
 0
 1
 2
 3
 4
 5
 6
 7
 8
 9

TO H.T.
 (POWER SUP)



COMPONENT REFERENCE

- * LF & MF RING
- ▲ HF RING
- ⊙ LF, HF & MF RING

TO H. T. U.
(POWER SUPPLY)

6.5 TRIPLE DECADE CIRCUIT**RESISTORS (RRC type 5SWD18 5%)**

<i>Circuit Ref.</i>	<i>Value</i>	<i>Type</i>	<i>Part No.</i>
R1 to R24	1.2K		2087
R25 to R96	10K		11503

CAPACITORS

C1 to 48	220pF	Lemco 310K	2588
----------	-------	------------	------

SEMICONDUCTORS

VT1 to VT24	Texas D535	3610
MR1 to MR35	Hughes HG1087	17956

6.6 SINGLE DECADE CIRCUIT**RESISTORS**

<i>Circuit Ref.</i>	<i>Value</i>	<i>Type</i>	<i>Part No.</i>
R1-R8	1.2K		2087
R25-R32	10K		11503
R49-R56	10K		11503
R73-R80	10K		11503

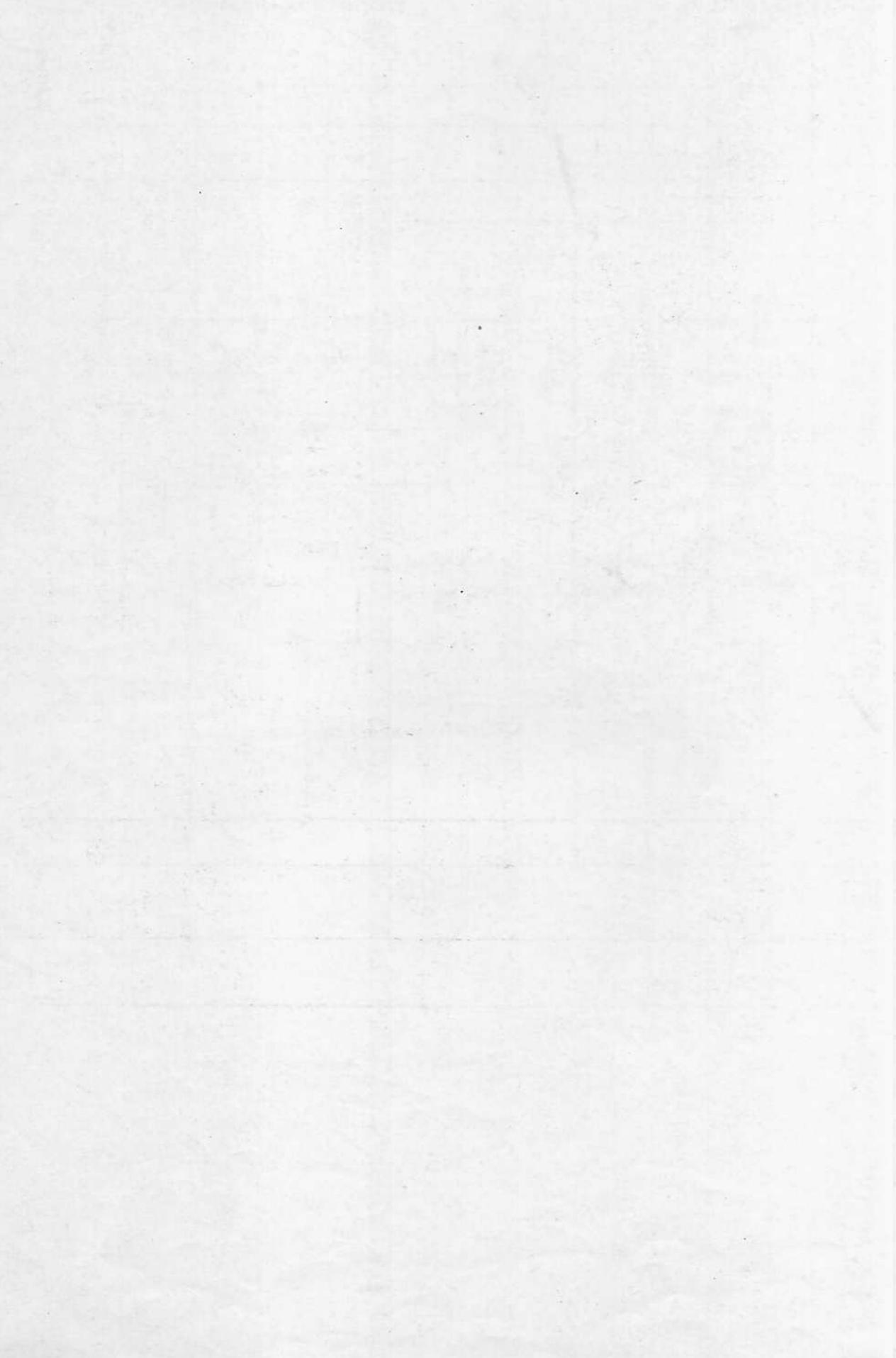
CAPACITORS

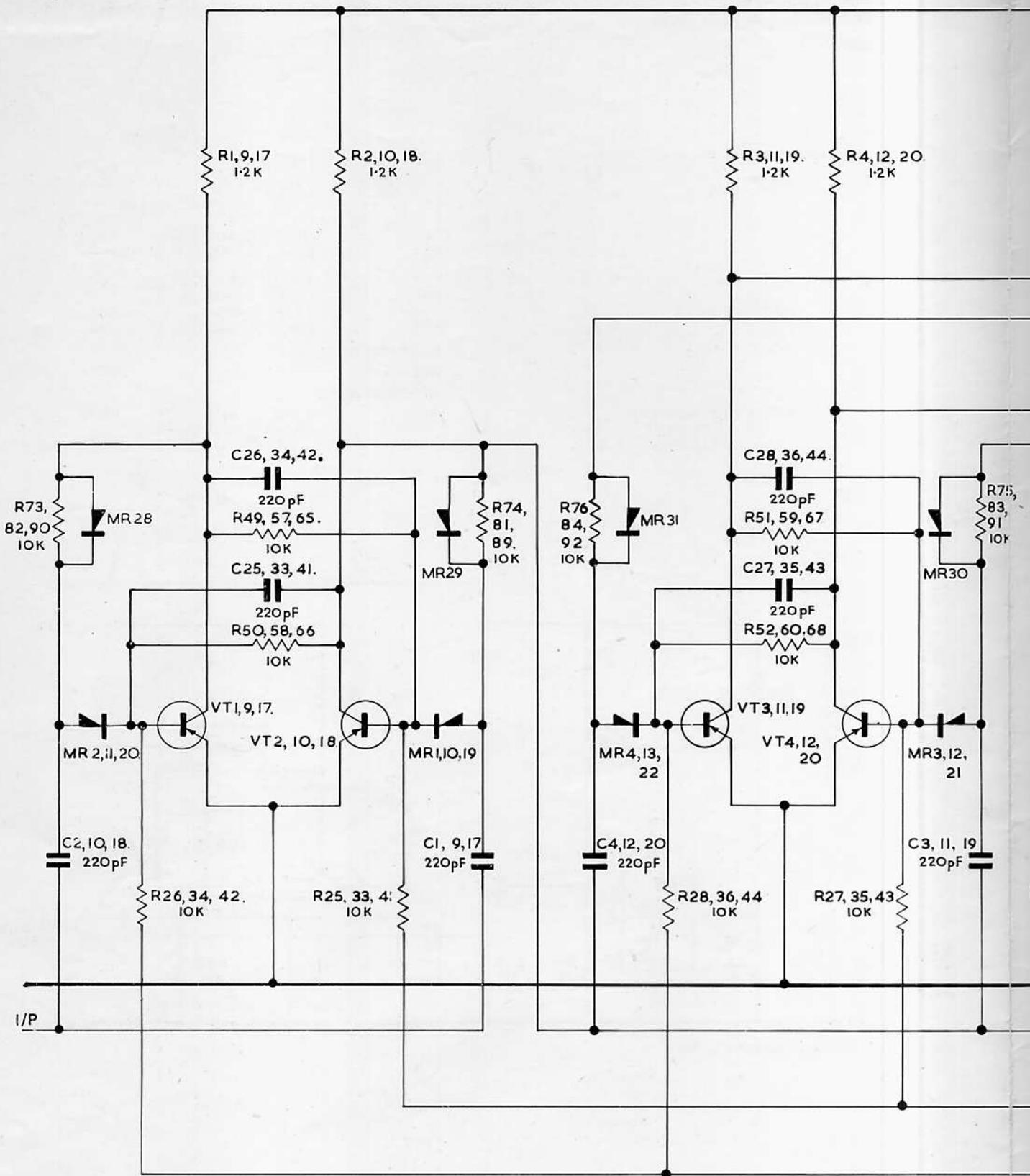
C1-C8	220pF	Lemco 310K	2588
C25-C32	220pF	Lemco 310K	2588

SEMICONDUCTORS

VT1-VT8	Texas D535	3610
MR1-MR9	Hughes HG1087	17956

Fig. 11 Triple and Single Decade Circuit





NOTES

1. DIODES MR28 - MR35 INCL. ARE ONLY FITTED ON FIRST DECADE OF EACH BOARD. THEY ARE NOT FITTED ON SINGLE DECADES.
2. CODING IS SHOWN FOR THREE DECADES PER BOARD.
3. RE-SET AND BIAS ARE INTERCHANGED AS REQUIRED TO RESET BOARD TO APPROPRIATE REQUIREMENT

R4, 12, 20.
1.2K

R5, 13, 21.
1.2K

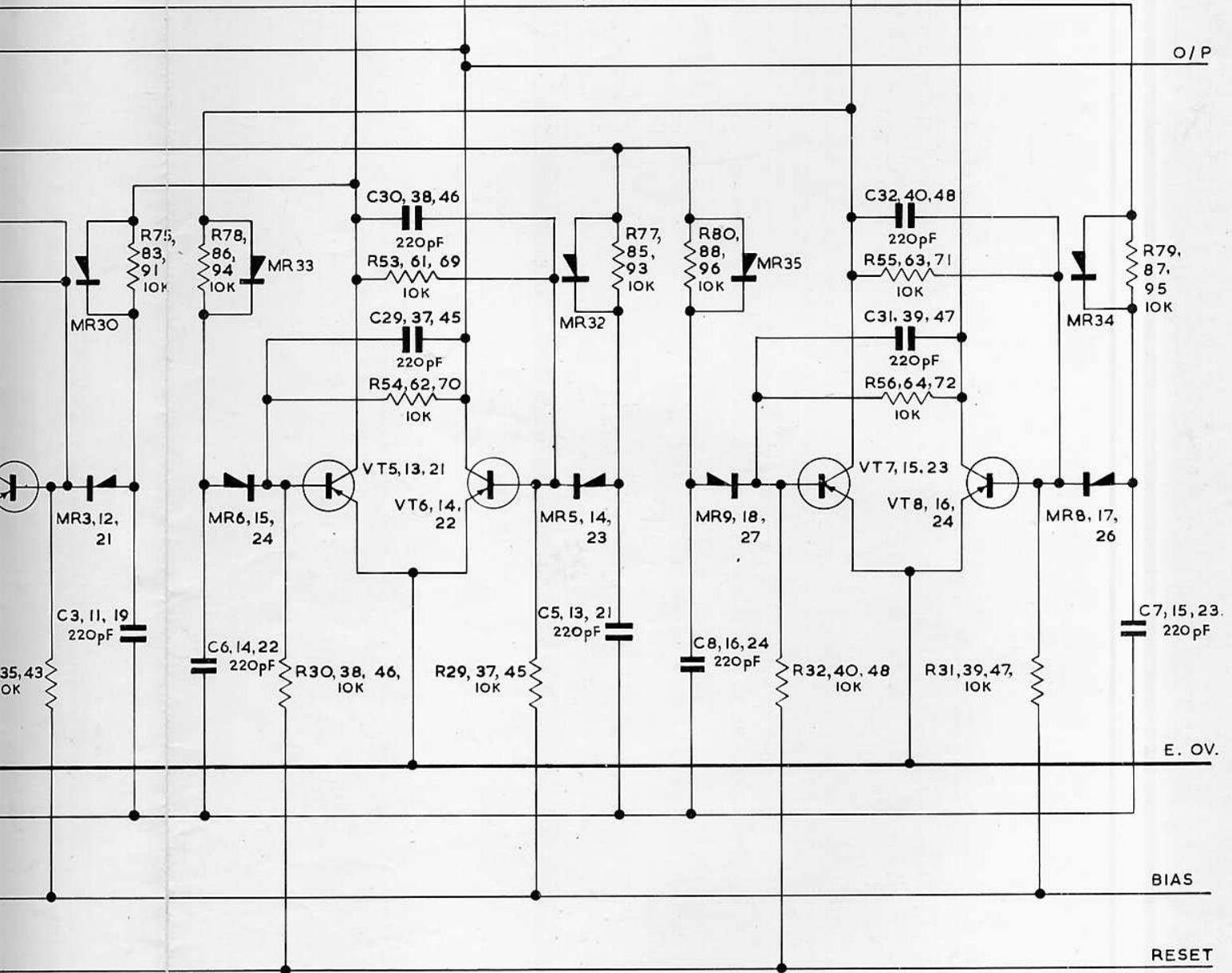
R6, 14, 22.
1.2K

R7, 15, 23.
1.2K

R8, 16, 24.
1.2K

MR7, 16, 25.

O/P



6.9 PRINTER ADAPTOR

RESISTORS (5% 1/8W cracked carbon, unless specified)

Circuit Ref.	Value	Type	Part No.
R1	2.2K		425
R2	100		111504
R3, 8	2.2K		425
R9	82K		2088
R10	1.2K		2087
R11	10K		11503
R12	1.2K		2087
R13	8.2K		314
R14	560		308
R15	8.2K		314
R16	22K		1544
R17	1.2K		2087
R18	6.8K		313
R19	1.5K		385
R20, 21	10K		11503
R22	4.7K		386
R23, 24	10K		11503
R25	4.7K		386
R26, 27	10K		11503
R28	47K		386
R29, 30	10K		11503
R31	4.7K		386
R32, 33	10K		11503
R34	4.7K		386
R35, 36	10K		11503
R37	4.7K		386

CAPACITORS

Circuit Ref.	Value	Type	Part No.
C1	25μ	15V Wima printilyt	17997
C2	0.047μ	160V Mullard	
		AA/A 10%	792
C3	680p	Lemco 310K 10%	
		T/E	3299
C4, 5, 6	33p	Lemco 310 NPO	
		10% T/E	4768
C7	0.047μ	Lemcolac 1212K	
		W/E	2793
C8	0.01μ	Lemco +50-25%	3312
C9, 14	680p	Lemco 310K 10%	
		T/E	3299

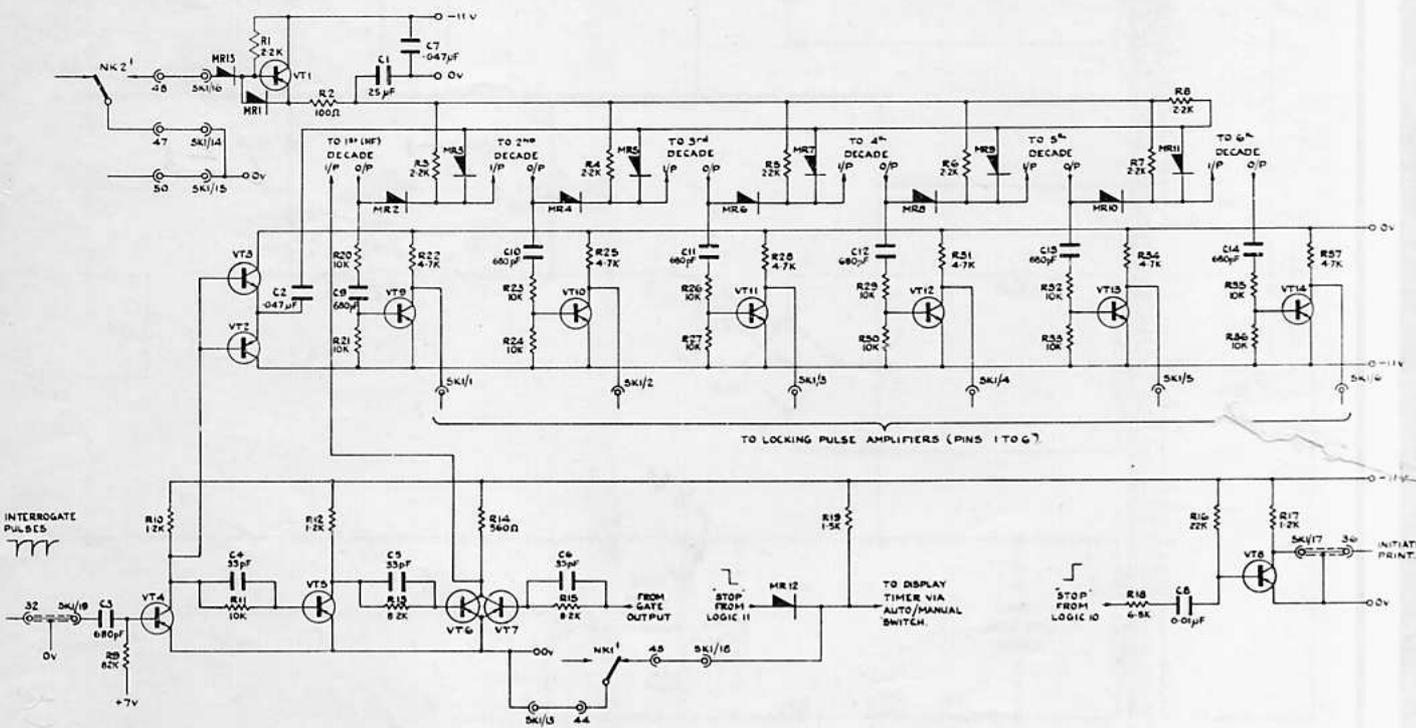
TRANSISTORS

VT1, 2, 4, 8	D535	Texas	or	3610
	GET889	Mullard		3607
VT5, 6, 7	V405A	Fairchild		19689
VT3, 9, 14	*U2275/1	Fairchild		20495

DIODES

MR1	1S920	Texas		2542
MR2-13	OA91	Mullard	or	2490
	HG1087	Hughes		17956

*May be replaced by 2N706 or 2N708

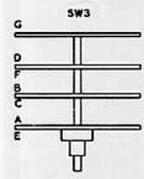
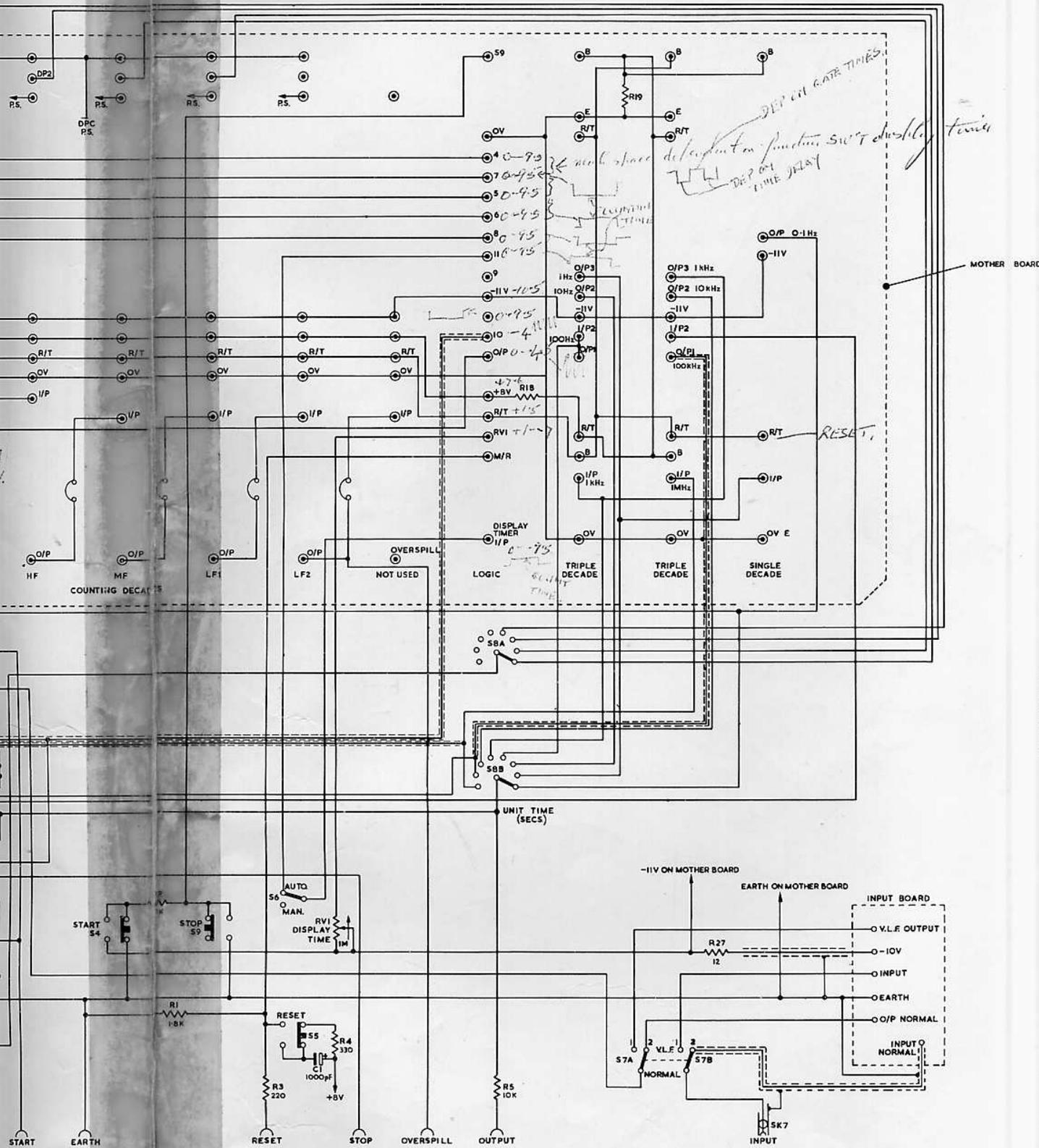


NOTE -
 1. 1st DECADE IS LEAST SIGNIFICANT, I.E. R.H. FIGURE
 2. FOR TCA & TCAA USE DECADE CONNECTIONS NUMBERED 1 TO 4.
 3. SK1 IS AT COUNTER END OF CABLE TO PRINTER.

Fig. 14 Printer Adaptor Circuit

Fig. 15 Interconnection Diagram





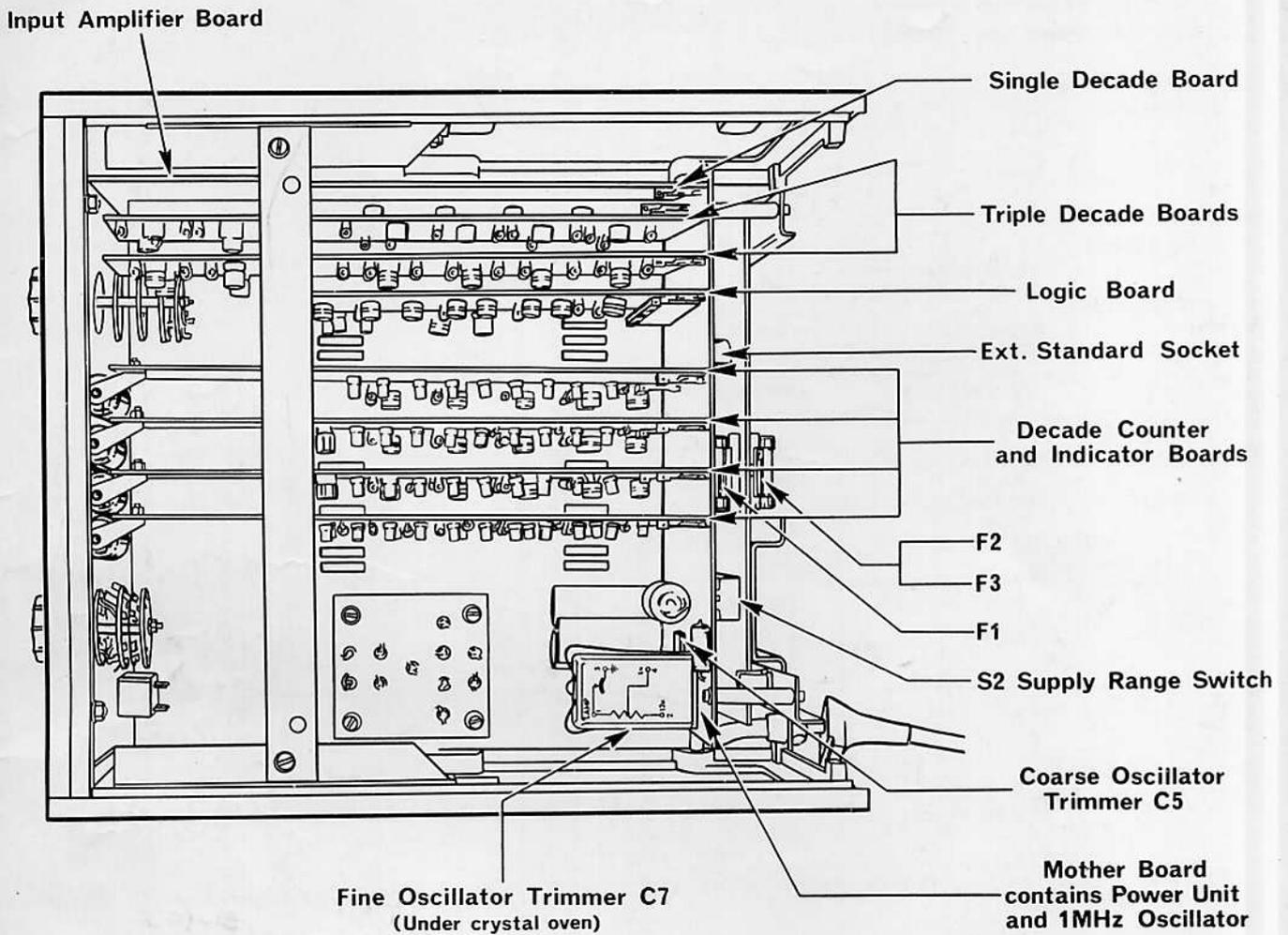


Fig. 16 Component Layout—Top View

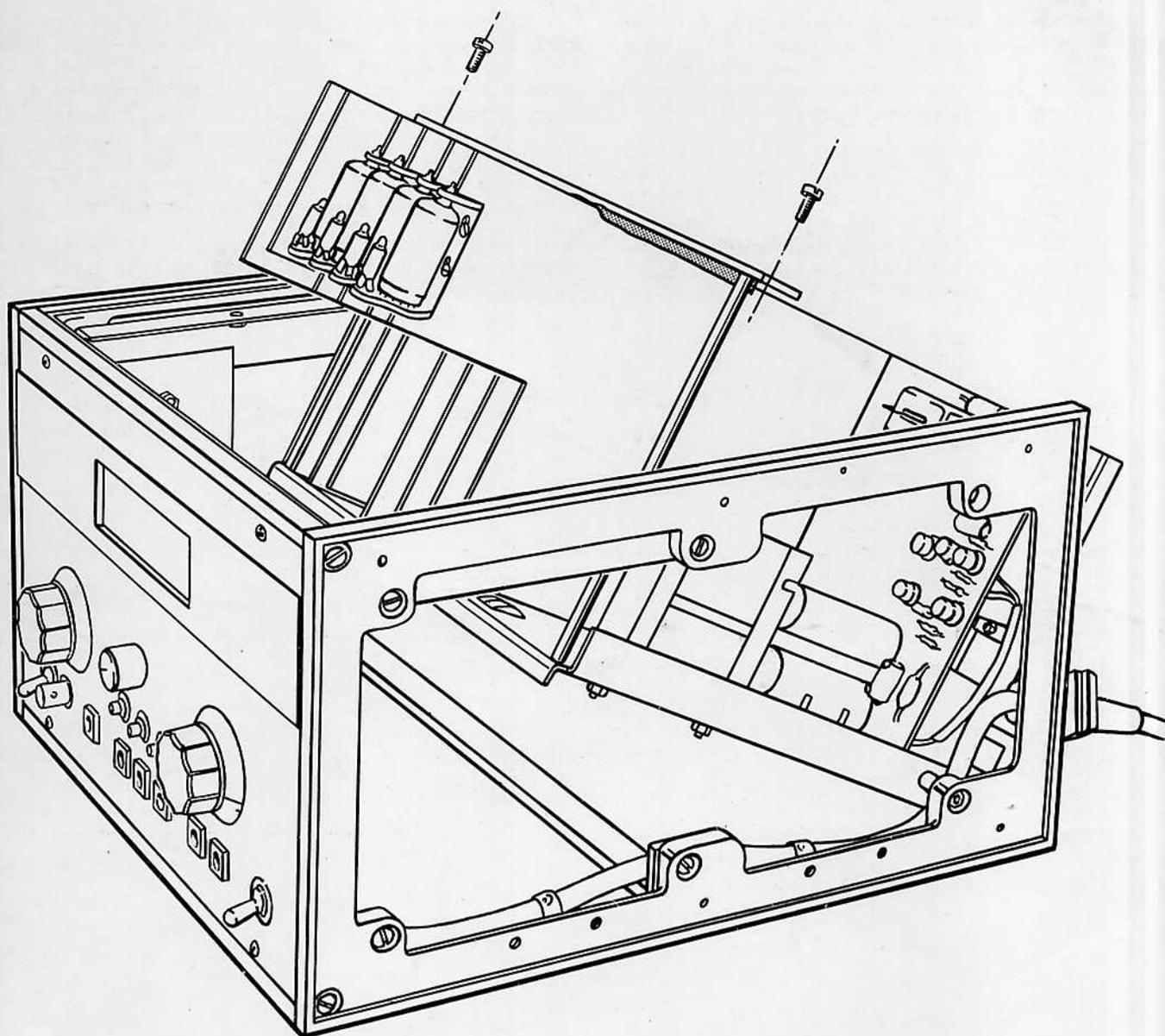


Fig. 17 Method of Access to Interior

This instrument is guaranteed for a period of one year from its delivery to the purchaser, covering the replacement of defective parts other than valves, semiconductors and fuses. Valves and semiconductors are subject to the manufacturers' guarantee.

We maintain comprehensive after sales facilities and the instrument can, if necessary, be returned to our factory for servicing. The type and serial number of the instrument should always be quoted, together with full details of any fault and the service required. The Service Department can also provide maintenance and repair information by telephone or letter.

Equipment returned to us for servicing must be adequately packed, preferably in the special box supplied, and shipped with transportation charges prepaid. We can accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired, the repair will be put in hand without delay and charged unless other instructions are received.

OUR SALES, SERVICE AND ENGINEERING DEPARTMENTS ARE READY TO ASSIST YOU AT ALL TIMES.