Introduction

Section 1

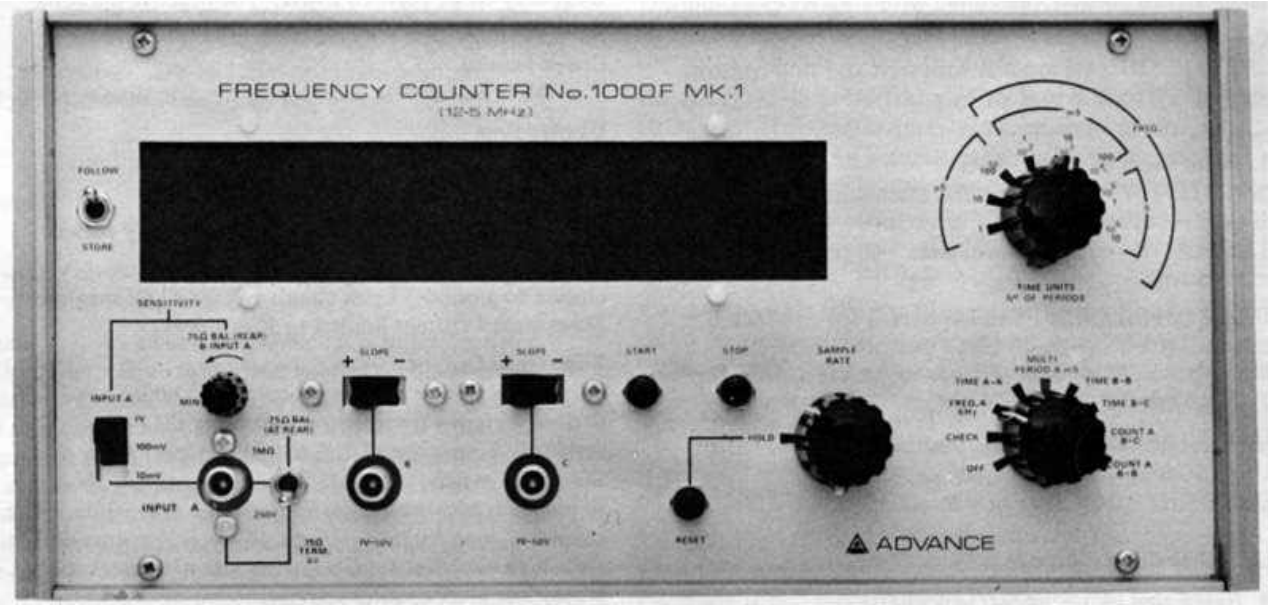
The 1000F Counter is a six digit instrument capable of measuring frequencies up to at least 12.5MHz with a maximum resolution of 0.1Hz. For higher resolution at frequencies up to 100kHz, a multiple period measurement facility is provided.

Input sensitivity is 10mV r.m.s. with a three position attenuator giving alternative sensitivities of 100mV and 1V, together with a 40:1 continuously variable attenuator. The input impedance is 1MΩ in parallel with 18pF, enabling the instrument to be used with standard oscilloscope probes. A 75Ω balanced input is also provided.

The internal 1MHz crystal standard enables a resolution of 1μS to be achieved on timing measurements and positive or negative slope selection on the B & C inputs allows direct measurements to be made of many waveforms (e.g. pulse widths). The B & C inputs may also be operated by contacts.

The indicator tubes used provide an extremely bright clear display, and the instrument uses integrated circuits for maximum reliability and space utilisation.

The instrument has a 'stored display' facility which provides a continuous display during measurements.



Specification Section 2

Display
The Counter has 6 in-line neon numerical indicators with decimal points for frequency and multiple period measurement. The display may be switched to "stored" or "direct".

FREQUENCY MEASUREMENTS
2Hz to 12.5MHz via input A with gate times of 1mS to 10S in decade steps. Decimal points automatically positioned to indicate kHz.

Time Measurement
Timing units from 1μS to 10S in decade steps. Start and stop inputs can be A to A (equivalent to single period), B to B, B to C or by push button.

Multiple Period
From 10 to 10^6 periods in decade steps within frequency range 2Hz to 100kHz. Measured with 100kHz clock units.

Count
2Hz to 12.5MHz via input A with start and stop controls via inputs B to B, B to C, or by push button.

INPUT A:
1. Front Panel (No. 1 Socket)
SENSITIVITY Three position attenuator providing 10mV, 100mV and 1V r.m.s. sensitivities, from 2Hz to 12.5MHz. A variable control gives >40 times reduction in sensitivity.

INPUT IMPEDANCE 1MΩ approx. 18pF, or 75Ω selected with a switch. In 10mV position, protective limiting reduces input impedance to 200kΩ approx. 120pF, with signals over 1V r.m.s.

MAXIMUM INPUT In 1MΩ position:–
Up to 20kHz 250V d.c. 250V a.c. r.m.s.
Over 20kHz 30V a.c. r.m.s. in 100mV and 1V position.
3V a.c. r.m.s. in 10mV position.
In 75Ω position 6V a.c./d.c.

2. Rear Panel (4mm 1/SSO/14 sockets)
Selected with switch.

SENSITIVITY 65 to 85mV, from 0.1 to 2MHz. Variable control gives >40 times reduction in sensitivity.

INPUT IMPEDANCE 75Ω balanced floating input, together with ground socket, and centre tap of balanced input.

MAXIMUM INPUT 6V a.c./d.c.

Inputs B and C
INPUT a.c. coupled, switched positive or negative slope selection.

SENSITIVITY 1.5V pk. Maximum input 50V r.m.s.

INPUT IMPEDANCE >5kΩ

FREQUENCY RANGE 100Hz to 1MHz

CONTACT OPERATION These inputs may be operated by contact closure (corresponding to a negative slope) or opening (corresponding to a positive slope).

FREQUENCY STANDARD
INTERNAL 1MHz crystal oscillator, oven controlled at +65°C. Set to 1 in 10^6 at +25°C. Stability ±5 in 10^6 from 0°C to +50°C, after one hour warm-up period.

EXTERNAL Via rear panel jack socket, coupled through 400V peak working blocking capacitor.

Sensitivity
Sine Wave 0.5V to 10V r.m.s. within frequency range 10kHz to 2MHz. Pulse 1V to 20V pk. to pk. within frequency range 10Hz to 2MHz. The negative duration must not be greater than 10 times the positive duration.

Check facility
The 1MHz Standard is counted for the gate time selected.

Display time
Continuously adjustable from 0.1S to 4S, or infinite.

Reset
INTERNAL Automatically at end of display period.

EXTERNAL By push-button or external contact closure to ground. Open circuit voltage +18V maximum. Short circuit current limited to 15mA peak.

Time Units Output
Pulses are available at a rear panel socket which are derived from the frequency standard via the decade dividers. Time units of 1μS to 10S are selected by the time units switch. Amplitude is approximately 2V pk to pk. from non-linear high impedance. A separate 1MHz output of approximately 2V pk. to pk. is also provided from high impedance, via a further rear panel socket and is available at all counter settings.

Power Supply
100 to 125V or 200 to 250V, 45 to 65Hz, 30VA.

Operating Temperature
0 to +50°C

Accessories Supplied
One miniature Jack Plug Part No. 2727
One Instruction Manual Part No. 30502.

Dimensions and Weight
11" (28cm) wide, 5¾" (15cm) high, 9⅞" (25cm) deep overall.
10½ lb. (4.8kg).

Operation

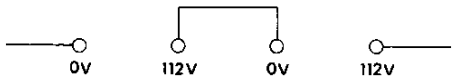
Section 3

3.1 PRELIMINARY

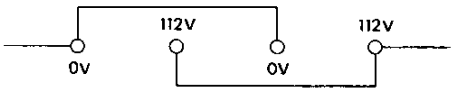
The instrument is normally despatched from the factory for use with a.c. supply voltages within the range 200V to 250V. To operate from a.c. supply voltages between 100 and 125V proceed as follows:–

Four taps are provided on the side of the supply transformer T1 nearest the top of the instrument, these are marked 0 – 112V 0 – 112V and enable the primary windings to be connected either in series (for 200V to 250V operation) or in parallel (for 100 to 125V operation).

The instrument is normally supplied for 200V to 250V operation with the windings connected in series, i.e. thus:–



To connect for 100V to 125V operation, remove the link and parallel the windings thus:–



Note that no connections to the other tags on the transformer must be made or disturbed.

When the instrument is despatched it is normally fitted with 2.5 amp. fuses in the fuse holders on the rear panel which are suitable for 200-250V operation. However 4.0 amp fuses should be fitted for 100-125V operation to prevent the fuses from being blown with the switch-on surge. The supply on-off switch is operated by the function switch, and when the instrument is connected to the supply and switched to the required function the neon indicator tubes will be illuminated.

3.2 INTERNAL STANDARD

Although the crystal oven begins to cycle, on and off, within a few minutes of switching on the counter, the maximum standard accuracy is only achieved after a period of one hour. At an ambient temperature of 25°C an accuracy of 3 parts in 10^6 is obtained typically within 20 minutes.

3.3 DISPLAY AND RESET

When the SAMPLE RATE control is switched to the HOLD position, reset may be actuated manually by the push button or by a closed contact to ground at the external reset socket which is located on the back panel. Repetitive readings are obtained by turning the control clockwise. The length of time for which a reading is displayed depends on the setting of this control and may be varied from at least four seconds to les less than 0.1 seconds when the control is fully clockwise, at the maximum sample rate.

The use of longer display times is advisable with measurements having a gate time longer than about 0.01 sec., since a very rapid sampling rate (short display time) makes it difficult to observe the steady display during the period when the gate is closed, unless stored display is selected.

3.4 STORED DISPLAY

When FOLLOW is selected, the display changes with the count and remains static only during the period set by the SAMPLE RATE control. When STORE is selected, the display will change at the end of each counting cycle (i.e. a 'stop' signal) and will be held static until the next counting cycle is completed.

3.5 FREQUENCY MEASUREMENT

The frequency of signals in the range 2Hz to 12.5MHz can be measured within the sensitivities specified in Section 2, either using the No. 1 input socket switched to 1MΩ or 75Ω input impedance or the balanced 75Ω input at the rear. (0.1 to 2MHz). The input attenuator should be used with larger signals as appropriate, in the 100mV or 1V position when using the front panel input. This will also enable inputs up to 30 volts, above 20kHz, to be measured. The input impedance of 1MΩ and 18pF enables a normal oscilloscope probe to be used. The variable sensitivity control can be used with both inputs.

The GATE TIMES switch shows five gate times: 10^{-3}, 10^{-2}, 10^{-1}, 1 and 10 seconds. In each case the display indicates kHz with an automatically positioned decimal point. The longer gate times can be used to obtain a greater number of digits and thus greater accuracy. For greater accuracy below about 100kHz it is advisable to select MULTIPLE PERIODS.

A greater number of digits than six can be resolved by taking two measurements, one measurement to obtain the most significant digits and another to obtain further digits, while overspilling the most significant ones by using longer gate times.

NOTE that an external standard is necessary to achieve greater accuracy than 1 in 10^6.

3.6 PERIOD MEASUREMENTS

3.6(a) TIME A-A

For single period measurements. To obtain an accurate determination of lower frequencies, it is better to measure the period of the signal, that is, the time elapsing between two consecutive negative going signals exceeding the triggering threshold. This is performed when the selector switch is set to TIME A-A.

The setting of the TIME UNITS switch determines the units of the display and it is necessary to take the reciprocal to obtain the frequency. For example using microsecond units (TIME UNITS 10^{-6} secs) a reading of 200,000 ±1μS gives a frequency of 5Hz ±0.0005%.

However, any period measurement suffers from a trigger point error due to hum and noise on the signal, causing the trigger point at which measurements are made, to jitter in time. Use of maximum sensitivity may reduce this error. However very noisy signals may cause spurious triggering, in which case the signal should be attenuated.

Particularly when using the 100mV or 10mV positions, care should be taken that spurious signals are not picked up, (with unscreened leads for example).

3.6(b) MULTIPLE PERIOD

The time indicated on the counter is always in millisecond units, and is the time elapsing between the first

Operation Section 3

positive going signal to trigger the counter and a selected subsequent positive signal.

The selection of the latter signal is made according to the NUMBER OF PERIODS selected, which may be from ten to a million, in decade steps.

On MULTIPLE PERIODS x 10^4 the accuracy achieved at 50kHz, for example, is ±0.0005% (neglecting any trigger point error) and accuracy increases progressively with greater number of periods and with lower frequencies.

3.7 TIME MEASUREMENTS

In addition to the TIME A-A function, time measurements can be made in three modes:–

3.7(a) TIME B-B

The TIME UNITS selected are counted between the first and second positive or negative going signals at the 'B' INPUT socket as selected by the SLOPE switch.

Subsequent pulses have no effect until reset has been applied.

3.7(b) TIME B-C

In this position of the FUNCTION SWITCH, the selected TIME UNITS are counted between the application of a negative or positive going signal at the 'B' INPUT socket and a subsequent negative or positive going signal at the 'C' input. The SLOPE switches select either negative or positive going signals to trigger the counter, as required.

The counter does not respond to any signal at the 'C' input before the signal at 'B' or any subsequent signals before the next reset is applied.

Both 'B' and 'C' inputs can be activated by a closed contact to ground and contact bounce may be suppressed by a capacitor of the order of 0.01μF connected across the contacts. The 'B' and 'C' inputs are a.c. coupled and therefore waveforms having a very uneven mark-space ratio may not trigger the counter on the positive edge of a narrow negative pulse or the negative edge of a narrow positive pulse.

3.7(c) MANUAL

In the TIME and COUNT position (see 3.8) the manual START and STOP push buttons may be used to control the gate. Reset must be applied before the buttons are operated again.

3.8 COUNTING

This function is similar to the TIME B-B and B-C functions except that the number of cycles of any signal at the A input socket is counted between start and stop signals. These start and stop signals may be applied in any of the ways detailed for the time measurement. The display should be switched to FOLLOW if the progress of the count is to be followed.

3.9 COUNTING PULSES FROM P.C.M. ERROR DETECTOR

Set the store/follow switch to follow, switch the A input attenuator to the 1 volt position. Select rear 75Ω balanced I/P, Count A, B-C and switch the sample rate control to the Hold position. Connect the Error Detector Balanced Output with a short, balanced screened lead to the 75Ω and chassis connections on the rear panel of the counter. With an output from the error detector, after pressing the counter Reset and Start buttons, the counter will register counts if the sensitivity is turned up. In order to reduce the possibility of interference the sensitivity control should be turned down to a level such that it is only about 45° higher than the minimum operate level. The a.c. supply lead should be positioned away from the signal leads and sockets and the apparatus positioned several feet away from other apparatus which might radiate interference, or a.c. operated equipment. Do not leave any leads connected to the front panel inputs.

3.10 CHECK

This facility enables the counting and time base decades to be checked. When the function switch is in this position, the standard frequency is counted for a time selected by the time units switch. In the 1 or 10 second gate position the counter should display 000000 ±1 count (i.e. 999999, 000000, 000001). The SAMPLE RATE control should be set anticlockwise to enable the display to be seen. When the instrument is first switched on it may not count correctly until a reset pulse is applied, since the decades may not start at zero count state.

NOTE. Check that the EXT. STANDARD jack plug has been removed, since this cuts off the internal standard.

3.11 REAR PANEL SOCKETS

3.11(a) EXTERNAL STANDARD

This input can be used to increase the acuracy or change the scale of measurements. Inserting a jack in this socket automatically disconnects the internal 1MHz standard. Inputs should be as specified in SECTION 2; with positive pulse inputs, the mark-space ratio should not be greater than 10 to 1.

3.11(b) 1MHz OUTPUT

Pulses are available from the internal standard of 2V pk-pk approximately, irrespective of the various control settings.

3.11(c) TIME UNITS OUTPUT

These pulses of approx. 2V pk-pk can be selected by the TIME UNITS switch, to occur at repetition rates in decade steps from 1μS to 10 Secs. They are not available in the multiple period and count functions, and the SAMPLE RATE control should be set to HOLD to prevent irregularity due to reset.

3.11(d) BALANCED OUTPUT

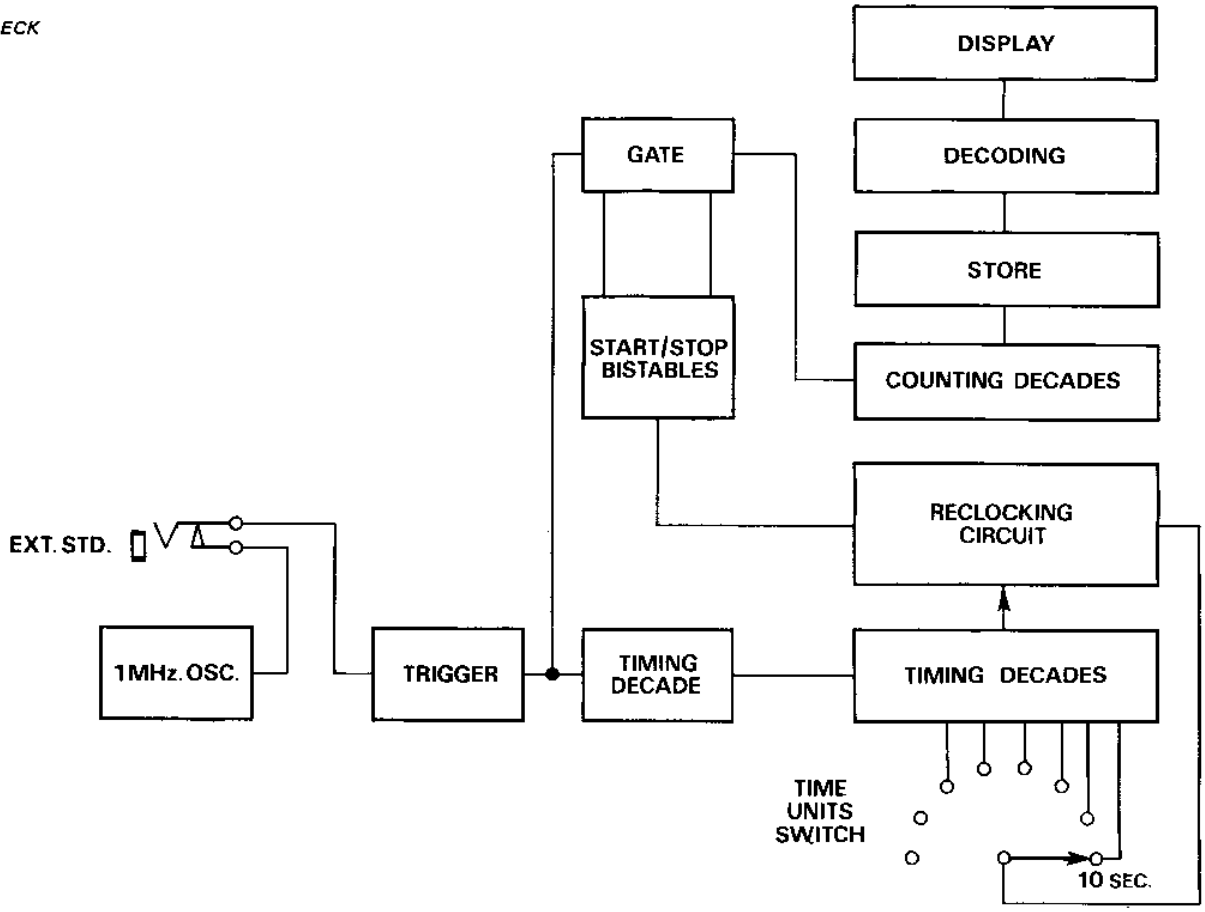
Use of the balanced input will reduce the possibility of stray interference signals being picked up. It is preferable to completely disconnect the front panel input to prevent very large signals being coupled in via stray capacitance in the 3 position input selector switch. A screened pair should be used to connect to this input and the screen connected to the ground socket. If possible the sensitivity control should be turned down, to further reduce the possibility of unwanted signals being counted. This input may be used (from 100kHz to 2MHz) in place of the A input in any function.

3.12 ROUTINE TESTING

The CHECK function may be used to test the operation of most of the circuitry, but for accurate frequency measurement the internal standard should be adjusted by reference to a known frequency. See Section 5.2 for procedure.

Operation Section 3

(a) CHECK



(b) FREQUENCY

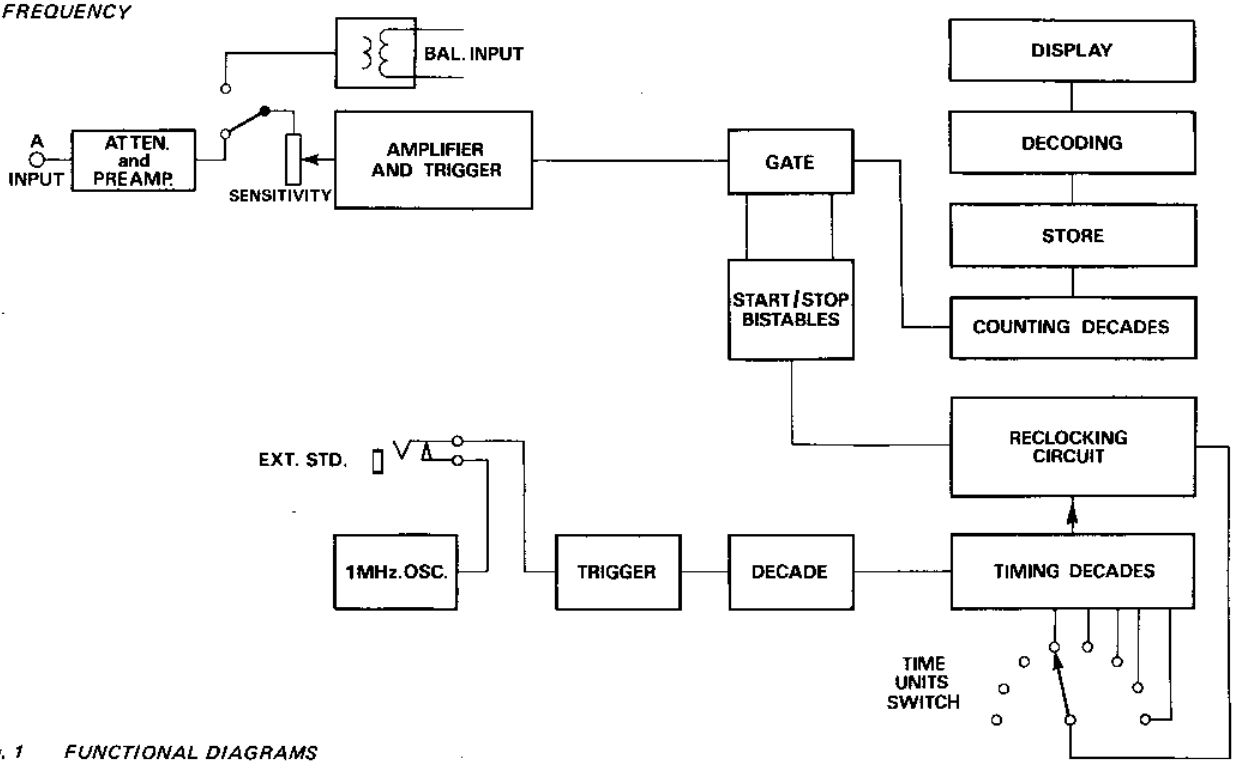
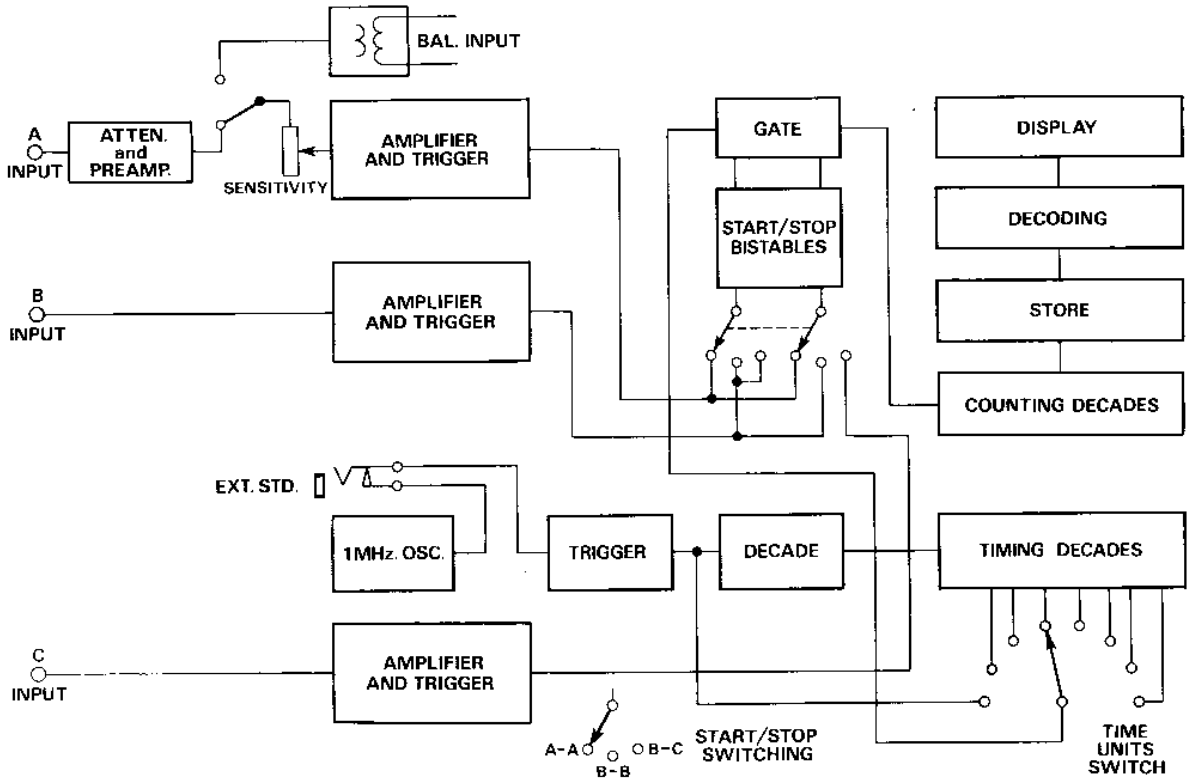


Fig. 1 FUNCTIONAL DIAGRAMS

Operation Section 3

(c) TIME



(d) MULTI PERIOD

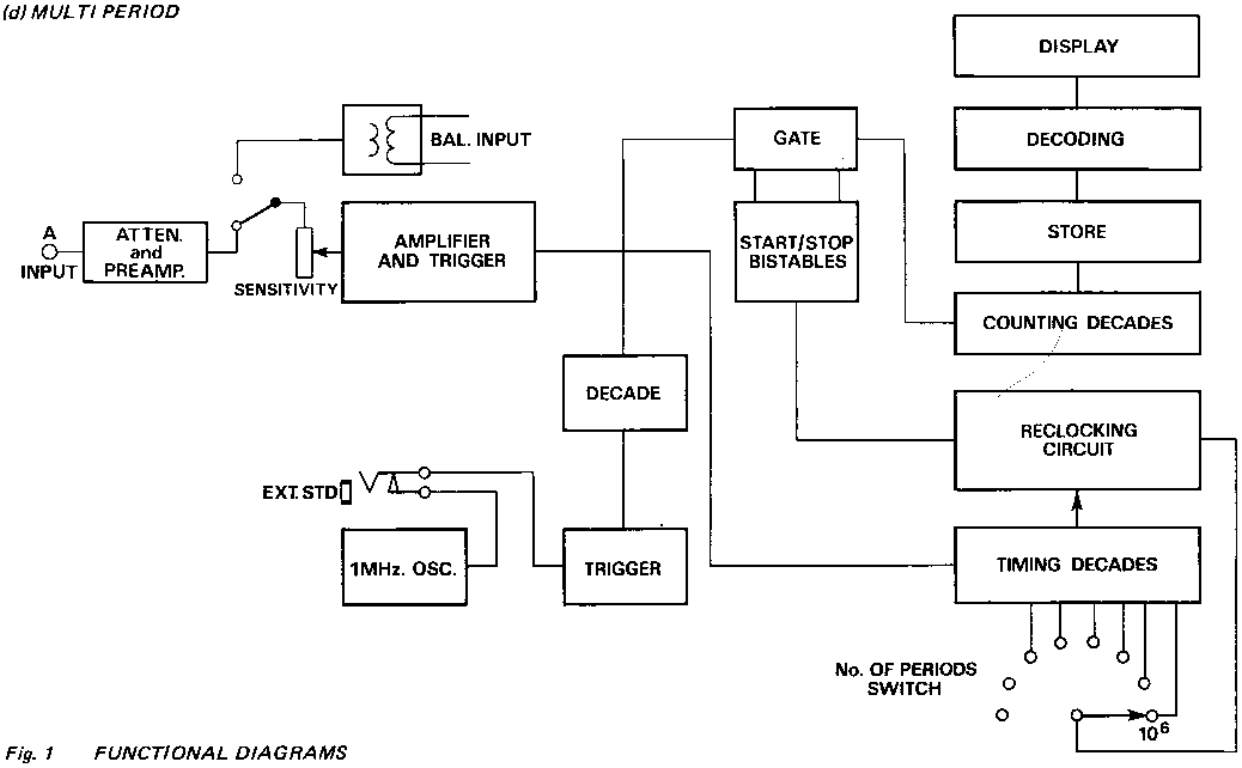


Fig. 1 FUNCTIONAL DIAGRAMS

Operation Section 3

(e) COUNT

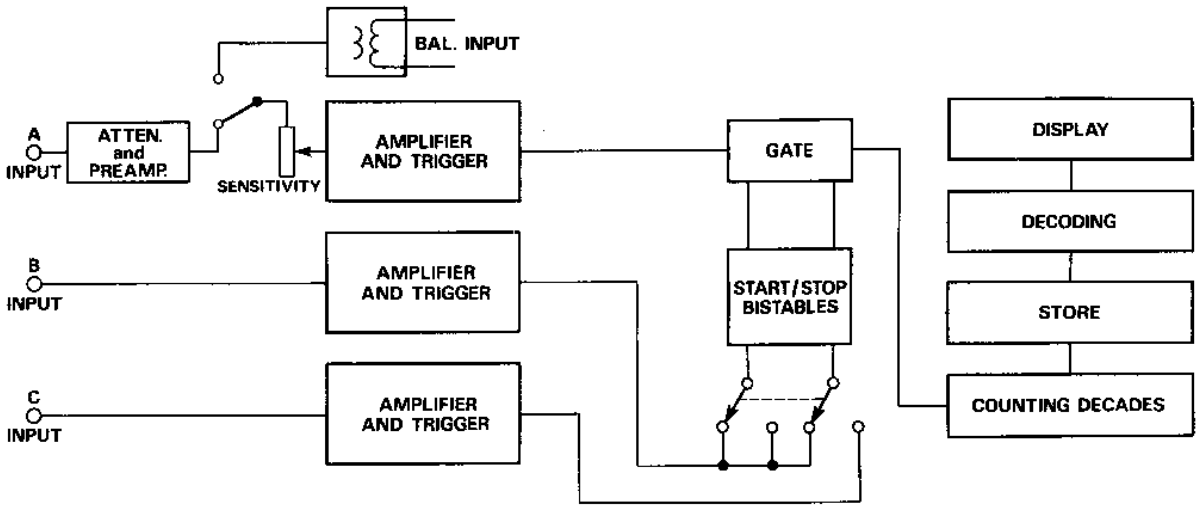


Fig 1. FUNCTIONAL DIAGRAMS

Circuit Description Section 4

4.1 GENERAL

The circuits of the instrument fall into three main sections: the counting decades and display, the timebase and the input amplifiers. A large part of the circuitry consists of integrated circuits and only the function of these will be described and not their internal circuitry. (See Section 5.4).

Block diagrams of the interconnection of the various circuits for different functions are to be found at the end of section 3. Fig. 1.

4.2 INPUT CIRCUITS

4.2(a) 'A' INPUT CIRCUIT (Fig. 3).

The input signal at socket A is amplified by the input amplifier and converted to square waves by the trigger circuit.

The input signal is fed through the switched attenuator to the high impedance field effect transistor stage, TR1, which is biased by a constant current stage, TR2. Protection against excessive negative signals is given by D1 and large positive signals are limited by TR1 itself together with R4 and R5. The signal is coupled by the emitter follower stage, TR3, via the input selector switch S10 and the sensitivity control, R44, to the three stage transistor amplifier, TR4, TR5 and TR6. DC feedback over these three transistors stablises their operating bias. Capacitors, C17, 20 and C21, maintain a level response at high frequencies.

The trigger circuit, TR7 and TR8, is a bistable type and TR9 is used to drive into subsequent circuitry without loading the bistable excessively.

4.2(b) BALANCED INPUT CIRCUIT

The Balanced Input circuit (Fig. 7) has 3 toroidal windings: a mutually coupled winding T2 acting as a longitudinal mode impedance; the primary T3, bifilar wound for good balance, and the unbalanced secondary T4. A single loop between the cores of T3 and T4 formed by the securing bolt and a wire link ensures very low unwanted coupling due to capacitance between windings, since the loop is grounded and passes through a screen. A trimmer, C78, corrects imbalance in the windings and input socket arrangement.

4.2(c) 'B' AND 'C' INPUT CIRCUITS (Fig. 6)

The B and C input amplifiers and trigger circuits are identical and therefore only the B input circuit will be described.

Transistor, TR1 forms a buffer and phase splitting circuit giving approximately unity gain. The SLOPE switch selects either the inverted signal from the collector or non inverted signal from the emitter, to drive the bistable trigger circuit formed by TR2 and TR3. This circuit is normally held by R4 with TR2 on and TR3 off, so that a negative going signal on the base of TR2 triggers the bistable. This gives a negative going edge at the collector of TR3 which is fed to the Start/Stop bistable circuit.

4.3 COUNTING AND DISPLAY CIRCUITS (Fig. 4)

4.3(a) START-STOP GATE

The pulses which are to be counted are fed via amplifier TR1 and differentiated by C2/R3.

The transistors, TR2, TR3 and TR4, form a gate which is controlled by the two bistable circuits, IC1 and IC20, which operate as follows:– (See also Table 4.2).

Initially, after reset, the two '0' outputs are at the logic '0' level which is 'high' and the output from the 'start' bistable, IC20, therefore switches on TR4 and closes the gate.

A negative going pulse at the clock input 'T', of the start bistable causes it to toggle since there is a low (1) level on the clear 'C' input, but the high '0' level on the set 'S' input prevents any further action by this bistable, until it is reset. When this bistable has toggled, it removes the bias from TR4 and opens the gate.

Since initially the 'stop' bistable, IC1, has high '0' levels on both inputs 'S' and 'C', it cannot toggle until after the start bistable has toggled and changed the 'C' input to a low '1' level. Then a negative going pulse on the stop bistable clock input 'T', will cause it to toggle; the '0' high level on the set 'S' input prevents any further action until reset is applied. When the Stop bistable has toggled, it applies bias to TR3 and closes the gate. The Start and Stop buttons operate IC1 and IC20 at their 'direct set' terminals. While the gate is open, pulses can pass to the drive stage, TR23 TR24, via inverter, TR5.

4.3(b) HIGH FREQUENCY DECADES

Transistors, TR6 and TR7, form a bistable which divides by two the input pulse frequency. TR10/11, TR12/13 and TR14/15 also form conventional diode steered bistables, with a gate, TR8 and TR9, to give division by five. The circuit functions as follows:–

Initially after reset, transistors, TR11, 13 and 14 are conducting (bottomed); TR10, 12 and 15 are therefore cut off. Since TR14 is bottomed, it does not switch on TR9, so that as TR7 toggles from the initial cut off state to which it is reset, the first 4 pulses pass through to the bistable, TR10 and TR11. This bistable divides the signal by two and the output from TR11 is coupled to the bistable TR12 and 13, which divides by a further factor of two. At the fourth pulse from TR7 therefore, TR14 and 15 toggle and the gate, TR8/9 is closed. The next pulse from TR6 however, causes the bistable, TR14/15 to toggle again and the gate is therefore open again. Outputs from TR7, 10, 12 and 15 provide a binary coded decimal (BCD) output. The output from the first decade at TR15, is inverted by TR25 and fed to IC2.

Integrated circuits, IC2, 19, 22, 23 and 24, form the second decade. IC2 is a J-K bistable, (see Table 4.2) which divides the input frequency by two, since the two steering inputs S and C are open, i.e. connected to the '1' state, ground. The '1' output from IC2 is fed to the clock input of bistable, IC19, which has the C steering input open since IC24 has been reset to the '1' state ('1' output at 0V). The '1' output from IC19 drives the clock input of bistable, IC22, the steering inputs of which are permanently open. As can be seen from Table 4.1 after the sixth input pulse, the '0' outputs from IC19 and IC22 are at the '1' low level. This causes the output of the first gate, pin 7-IC23, to change to the high level and thus apply a low '1' level to the steering input C of IC24 via the second gate of IC23 which acts as an inverter. At the eight pulse, the negative going output from IC2 causes IC24 to toggle, and its '1' output now at the high '0' level, inhibits IC19 until after the tenth pulse. The tenth pulse causes IC24 to toggle back to the set state and all the bistables are then again in the '0' state.

Circuit Description Section 4

TABLE 4.1 DECADE COUNTING where '1' indicates the bottomed state and '0' the cut off state.

Input Pulse No.	TR7 or IC2 BCD '1'	TR10 or IC19 BCD '2'	TR12 or IC22 BCD '4'	TR15 or IC24 BCD '8'
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0
11	1	0	0	0
12	0	1	0	0
		etc		

TABLE 4.2 J K BISTABLE LOGIC
Output State after application of negative going pulse at the clock input (pin 3)

Set (Pin 2)	Clear (Pin 4)	'1' Output (Pin 9)
0	0	X^n
0	1	0
1	0	1
1	1	X^{-n}

0 = High 1 = Low X^n = output state prior to clock pulse i.e. does not toggle.

4.3(c) INTEGRATED DECADES AND DISPLAY

The positive going edge of the BCD '8' output from the second decade drives an integrated circuit decade, IC3. The BCD '8' output of IC3 drives IC4 and so on, to IC6.

The 1, 2, 4 and 8 outputs from each decade are fed to a buffer-storage unit (IC13-18) which consists of four gated. latch circuits and a common gate drive. Information which is present at the four data inputs enters the latches throughout the period of 0V enter-command applied to the gate input terminal. With the gate voltage positive, the information is stored until a subsequent enter-command permits a change.

The enter-command pulse is derived from the 0 output of the STOP bistable, IC1. When the STOP signal occurs this output provides a negative-going edge which is differentiated in C36/R37 to provide a negative pulse to the first part of IC21. The output from this is coupled to both inputs of the second part of IC21 to provide an output with maximum fan-out.

When FOLLOW is selected by the front panel switch the enter-command line is grounded and the latching circuits then follow each change in the data.

The latched BCD output from the buffer-storage units provides the drive to the decimal decoder units IC7-12. These convert BCD data to decimal data and provide the drive required for the cathodes of the neon number tubes in the display.

Decimal point switching is carried out by the function and time unit switches for frequency and multiple period measurements.

4.3(d) RESET PULSE GENERATOR

The reset circuit which resets all decades to zero at the end of the display period functions as follows:—

When the sample rate control is switched from the 'hold' position, a charging current can flow through it into C33, after a stop pulse has triggered the stop bistable, IC1, and cut off TR19. The charging rate is determined by the setting of the sample rate potentiometer. As C33 charges, it switches on TR18 and causes TR20 to cease conducting. TR20 is directly coupled to TR21 and the switching action re-generates through R64 so that a positive reset pulse occurs on the reset line from the collector of TR21. TR22 acts as a buffer to supply the reset pulse to the integrated circuits.

The reset pulse resets the '0' output of the stop bistable of IC1 to the 'high' stage and bottoms TR19 which therefore discharges C33 through R59, and C32 charges through R61 and R64 giving a reset pulse length of approximately 0.7mS.

The circuit of TR17 enables manual reset to be applied.

Circuit Description Section 4

4.4 TIMEBASE AND POWER CIRCUITS (Fig. 2)

4.4(a) 1MHz OSCILLATOR

Crystal XL1, TR8 and TR9 form the oscillator circuit, positive feedback occurring between the emitter of TR8 and the emitter of TR9, through XL1.

At the series resonant frequency of the crystal therefore, when its impedance is lowest, the positive feedback is greatest and oscillation takes place.

The basic resonant frequency of the crystal is slightly below 1MHz and the series capacitors can be adjusted to raise the frequency to exactly 1MHz.

TR10 is an emitter follower stage which only lightly loads the oscillator stage. The output from TR10 is fed via the EXTERNAL STANDARD jack socket to the trigger circuit, TR11 TR12, which shapes the 1MHz, or the external standard frequency, into pulses suitable for driving the timebase.

4.4.(b) TIMEBASE

The timebase consists of seven integrated circuits decades which divide down the frequency in stages of ten, from 1MHz to 0.1Hz. The connection from the first to second decades is made via the function switch so that the decades, IC2-IC7, may be used to divide the input frequency in the multiple period function.

The circuitry comprised of IC8 and IC9 is used to re-clock the timebase to eliminate propagation errors when deriving start and stop pulses for the counter gate. The start and stop pulses are timed from the BCD '1' output from the second decade, IC2, as follows:–

Reset is applied to TR7 which clamps the output of one side of the bistable formed by the interconnection of two gate circuits in IC9.

The first positive going edge from the BCD '1' output of IC2 is amplified and differentiated by part of IC8 and appears as a positive going pulse at the upper gate circuit of IC9, pin 3, and causes it to toggle. The negative going output from the bistable is used as the start pulse.

The selected time unit pulses, switched by the TIME UNITS switch from a decade output are amplified and differentiated by the remaining circuitry of IC8 and positive going pulses are fed to the lower gate of the bistable, IC9. The first positive going edge occurs after a complete count of 10 by the appropriate decade and this resets the bistable so that the next positive going '1' output from IC2 can cause the bistable to toggle and give a negative stop pulse. These positive going '1' pulses are therefore gated by the required decade output to give an exact gate time.

Transistors, TR4 and TR5, form a gate which is closed during reset to prevent pulses passing into the decades during the reset period and TR6 inverts the signal so that the trailing edge of the reset pulse does not trigger the decade.

4.4(c) POWER SUPPLIES

TR1 is a series regulator transistor for the main power supply and is controlled by TR2 and TR3 from the reference zener, D5, to give a constant 5.4 volt supply. The integrated circuits are operated from a 3.8 volts supply obtained from the 5.4 volt supply by series silicon diodes, D3 and D4.

The 200 volts d.c. rectified output from D1 supplies the indicator tubes and is decoupled by R2, R3 and C2 together with zener diode, D6 to give a 20 volts supply with a minimum ripple, suitable for the input amplifier. A further 16 volt supply is obtained by rectifying and smoothing the crystal oven supply and is used to feed the display timer circuit.

Maintenance Section 5

5.1 GENERAL

5.1(a) REMOVAL OF CASE

The top and bottom covers may be taken off by removing the two screws at the rear of the instrument and sliding back the covers. If necessary the side covers can also be slid back when the two rear side trims, each retained by two screws, have been removed. The case should only be removed with the instrument power supply disconnected, to prevent accidental short circuits.

5.1(b) ACCESS TO COMPONENTS

The top (timebase) board of the instrument is hinged for ease of servicing and is retained by two screws at the rear.

The input amplifier screen is secured by five screws. The side cover should be removed to gain access to the upper fixings which are to the side plate if the top half of the screen is to be removed.

5.1(c) FUSE REPLACEMENT

In addition to the line supply fuses on the rear panel (see SECTION 3.1) there is a fuse in the stabilised supply, rated at 2.0 amp. and a 100mA fuse in the 200V supply adjacent to it.

5.2 OSCILLATOR FREQUENCY ADJUSTMENT

When the instrument is despatched from the factory, the oscillator will have been set for the greatest accuracy at room temperature. Ageing is a characteristic of crystal oscillators and this results in a slow drift of frequency. This slight drift is unpredictable and if the best performance is desired it is advisable to check against a standard frequency at periods of a few months and correct as necessary. A standard frequency having an accuracy of at least 1 part in 10 million is required, such as the Advance Off Air Frequency Standard OFS1B.

If the standard frequency is a multiple or submultiple of 1MHz, it can be displayed together with the 1MHz counter frequency from the rear socket, on an oscilloscope to form a Lissajous figure, or with one frequency viewed on a normal timebase triggered from the other frequency. Use the trimmers C17 (coarse) and C18 (fine) to obtain a stationary display. C19 may require changing if XL1 is changed. Alternatively adjust the trimmers to obtain the correct reading of frequency on a 10 second gate time, with a standard frequency greater than 100kHz.

The fine trimmer, which may be adjusted with the covers on the instrument, is accessible through the side cover at the rear of the left hand side of the instrument. Allow at least one hour for the instrument to warm up to maximum accuracy before carrying out the oscillator adjustment.

5.3 GUIDE TO SERVICING

5.3(a) POWER SUPPLIES AND BIAS VOLTAGES

The voltages measured at various points in the instrument, with function switch on CHECK and SAMPLE RATE set to HOLD are as follows:–

TABLE 5.1 OPERATING VOLTAGES

Fig. 2	TR1 emitter	+5.4V ±10% at 1.0 amps
Fig. 2	C3 or Test Link 1	+3.5 to 3.95 volts at 0.7 amps.

Other d.c. voltages should be within 20% of the values in the circuit diagrams. It is important to ensure that at no time more than +4V is applied to the integrated circuits and if a fault is repaired in the power supply circuits, the link on this board (See Fig. 8) can be removed and a dummy load of 15Ω 2 watt resistor connected to ground. The voltage across the resistor should not exceed 4V; the link may then be replaced.

5.3(b) FAULT LOCATION

When repairing the instrument the fault should be localised to a specific section of circuitry, where the faulty component can more readily be located. Table 5.2 gives a suitable procedure. Reference should be made to SECTION 4, Fig. 1 and circuit diagrams.

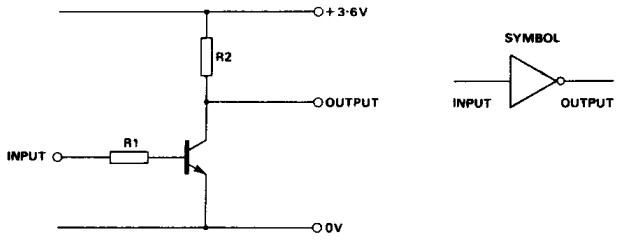
5.4 INTEGRATED CIRCUITS

The following additional details of integrated circuit operation are given to assist in fault location.

The Integrated circuits used are from two families, RTμL (Resistor Transistor Micro Logic) and CμL (Counting Micro Logic). The RTμL circuits are specified for operation with a power supply 3.6V ±10% and the CμL from 3.3 to 5.5V.

RESISTOR-TRANSISTOR MICROLOGIC RTμL

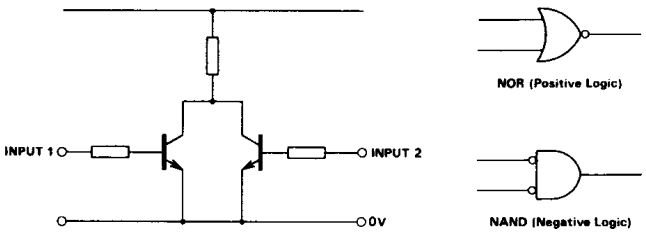
The basic building block of RTμL is a single inverting amplifier:–



If the input terminal of the amplifier is connected to 0 volt then the transistor will be non-conducting and the output voltage will be approximately +3.6 volts: the output is said to be high. If the input terminal of the amplifier is connected to +3.6V then the transistor will be conducting and the output voltage will be approximately 0 volt: the output is said to be 'low'.

The transistor is represented by the triangle in the symbol above – indicating an amplifier; its inverting action i.e. output low for a positive input, is indicated by the circle. Its function is to provide inversion, shaping and/or drive capability as a buffer amplifier (see note 1). The Quad Inverter RTμL927 has four such stages in its can.

A two input RTμL gate consists of two transistors connected in parallel:



Maintenance Section 5

If either or both of the inputs are connected to the +3.6 volt supply then the output voltage will be approximately zero volts due to the conduction of either or both transistors. The output is then said to be at a 'low' state.

If both inputs are held 'low' then the output voltage is approximately +3.6 Volts due to neither transistor conducting, the output is then said to be at a 'high' state.

The two input gate above is an inverting OR gate with HIGH inputs (POSITIVE LOGIC) and is called a NOR gate. It is also an inverting AND gate with 'low' inputs (NEGATIVE LOGIC) and is called a NAND gate. It thus has the two symbols above, the circle indicating inversion.

The RTμL flip-flop operates in the following manner:–

The application of a 'high' signal to the Reset input (8) directly controls the output of the flip flop such that the level at the output terminal Q (Pin 9) will be 'low' and at $\overline{Q}$ 'high'. A 'low' signal applied to the Reset line has no effect.

The application of a 'high' signal to the Set input (1) directly controls the outputs of the flip flop such that the level at the output terminal $\overline{Q}$ (pin 7) will be 'low' and at Q 'high'. A 'low' signal applied to the Set Line has no effect.

The Steer input acts as a gate on the clock pulse input. If the Steer inputs are held 'high' the clock pulses (Pin 3) have no effect. If the Steer inputs are held 'low' the clock pulses at Pin3 do have effect; each negative transition of the clock pulse will cause the flip-flop to change state. (see Note 2). If only one Steer input is held high the outputs will go to the states:–

Q – high $\overline{Q}$ Low for Steer input pin 2 high.

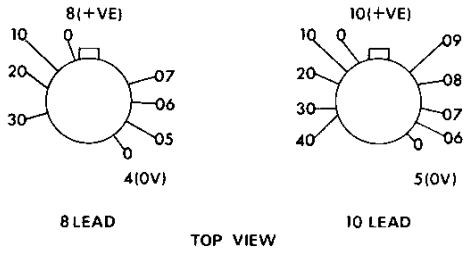
Q – low $\overline{Q}$ High for Steer input pin 4 high.

after the clock pulse.

Summarising:

	Outputs	
	Q	$\overline{Q}$
Reset H	L	H
Set H	H	L
Steer L	Change of State at each negative transistion of the clock pulse.	
Steer H	No change of State at a clock pulse.	

The integrated circuits used in this instrument are in a TO5 can but the leads have been arranged into a square configuration for ease of printed circuit board layout the pin numbering is as follows:–



NOTE 1: The output voltage of resistor-transistor micrologic depends upon the number of micrologic elements connected and the loading factor of the elements. Therefore in some cases the output voltage swing may be as low as 750mV.

NOTE 2: The RTμL flip-flop requires a fast negative transition to switch it (fall time should not exceed 100 nanoseconds).

TYPICAL OPERATING CONDITIONS AT 25°C

Circuit Type	Input Resistor	Output Resistor	Input High	Input Low	Power Dissipation
914 gate	450Ω	640Ω	>850mV	<460mV	40mW
927 inverter	450Ω	650Ω	>850mV	<460mV	80mW
926 flip flop	clock 300Ω others 600Ω	640Ω	>850mV	<460mV fall time 1-100nS clock	90mW
958 decade	2kΩ count 300Ω reset		>1.2V count input 1μS max. rise time.	<0.45V	140mW
959 latch	Gate 1K Data 2K	4K	>1.1V	<0.5V	115-135mW
960 decoder	2K	–	>1V	<.4V	45mW

Maintenance Section 5

COUNTING MICROLOGIC CμL. The Counting Micrologic consists of three types of circuits:

(i) Decade 958. This consists of four Bistable Flip flops interconnected so as to divide by ten, with a BCD output, similar to the discrete decade described in Section 4.3(b).
The output waveforms are shown in Table 5.3(a) having an amplitude of about 1.8 volts pk-pk. The Reset input, sets all outputs to the 'high' level state (0) since the counting circuits operate with negative logic.

(ii) Storage Circuit 959. This comprises four Bistable Flip flops with a common clock input.
Each bistable has one steer input which is used as a data input and the output follows this when the clock input is taken low (the clock, latch or strobe line is DC level operated).

(iii) Decoder, BCD to Decimal, 960. This circuit has 10 decimal outputs, one of which goes low when the appropriate BCD (–ve logic) code is applied to the inputs. The outputs are able to withstand an 'off' voltage of up to 50 volts, which would be at the 'off' cathodes of the numerical indicator tube.

Test	*Fault*	*Possible Cause*
Check supply tapping and supply fuses. Switch to CHECK. Switch to DIRECT Display.	No display	Failure of 200V supply
	All tubes blurred.	Failure of 5.4V supply (check FS4) or 3.8V supply.
Press reset button	Display not zero	Faulty reset circuit.
Display resets to zero but does not count, switch to 1μS TIME UNITS and TIME B-B, press RESET and START buttons.	Does not count	Fault in start-stop gate or logic. Fault in 1MHz oscillator, trigger or EXT STD socket. Fault on display board.
Switch to each TIME UNITS position in turn and check that counting occurs when RESET and START applied.	Does not count with longer TIME UNITS.	Faulty decade. Faulty part IC8. Fig. 2. Fault on display board.
Apply suitable input to socket A	Counts on CHECK and TIME B-B, B-C but not other functions.	Fault in input amplifier or trigger.
	Counts incorrectly	See next test.
Set Time Units to 1 sec. and Time B-B. Press RESET and START	Right hand digit does not count from 0 – 9.	Fault in transistor decade read out package, or storage IC13.
As above but 0.1 sec. TIME UNITS	Second digit does not count 0 – 9.	Fault in second decade storage or read out IC8 Fig. 4.
etc. up to 1μS		Faulty decade read out, or storage.
Apply known input frequency to socket A measure frequency	Incorrect frequency steady readings.	Incorrect triggering in input amplifier. Incorrect gate time – try other positions of TIME UNITS SWITCH to find faulty decade in timebase. Fault in re-clocking circuit of timebase. Incorrect standard frequency.
Frequency or Period measurements.	Erratic readings	Hum or noise on input signal, or input amplifier. Check for steady output from amplifier trigger circuit. Power supply ripple. Poor grounding or screening of input amp.
	Two digits on display tube	Incorrect (Not BCD) output from decade. Faulty read-out package. Faulty tube.
	Correct operation, on manual RESET but not SAMPLE RATE.	Display timer circuit fault.

TABLE 5.2 FAULT LOCATION

Maintenance

Section 5

Faults may also be caused by faulty switches, wiring or joints. Further fault finding may be carried out by using an oscilloscope.

The 1MHz standard should be traced with the SAMPLE RATE control in the HOLD position and function switch on CHECK or FREQUENCY, through the timebase decades, ensuring that they divide by ten.

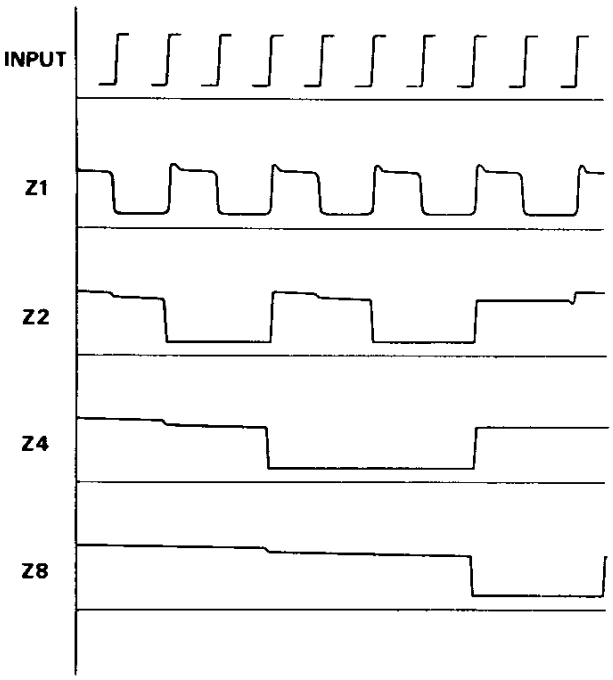
Checking the remaining circuitry is often most easily done using the COUNT function with a normal input signal: after the generation of RESET and application of manual START the counting gate should open and the counting decades may be checked.

Table 5.3 shows typical waveforms observed with a high performance oscilloscope and probe.

Trimmer C78 adjusted to give minimum output (below 2mV pk-pk) at the output of T4 with a 10V r.m.s. signal at 5MHz applied via matched 39Ω resistors as a common mode signal to the two 75Ω input terminals. The signal ground should be connected to the chassis connection.

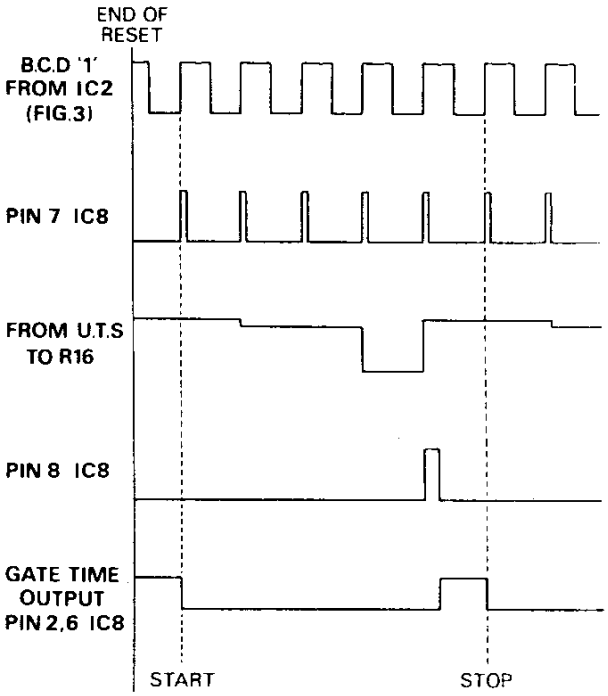
NOTE that when ordering spares the circuit reference and board assembly number should always be quoted in addition to the part number and value.

(a) BCD Decade Outputs



Note: The small steps in the waveforms are not significant.

(b) Reclocking Circuit.



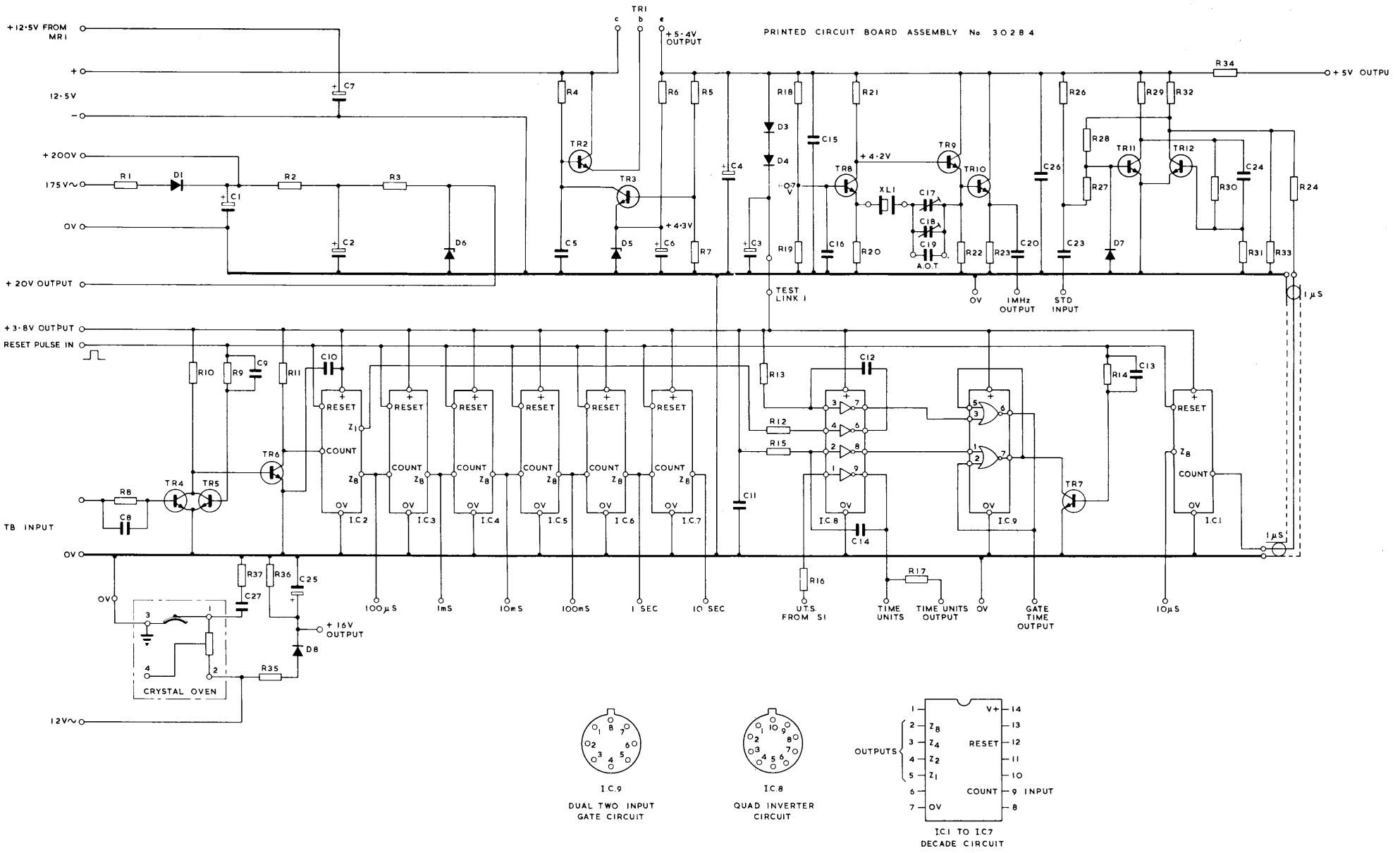
Shown with Time Units Switch set to 10^{-4} sec.

TABLE 5.3 WAVEFORMS

Component List and Illustrations Section 6

TIMEBASE & POWER SUPPLY CIRCUIT 1MHz

Ref	Value	Description	Tol %		Part No.
RESISTORS					
R1	330Ω	Metal Oxide MR5 or TR5	2	½W	28788
R2	15K	Cracked Carbon	5	1W	2051
R3	15K	Cracked Carbon	5	1W	2051
R4	820Ω	Cracked Carbon	5	⅛W	1637
R5	470Ω	Cracked Carbon	5	⅛W	1373
R6	1kΩ	Cracked Carbon	5	⅛W	384
R7	4.7kΩ	Cracked Carbon	5	⅛W	386
R8	4.7kΩ	Cracked Carbon	5	⅛W	386
R9	4.7kΩ	Cracked Carbon	5	⅛W	386
R10	1.8k	Cracked Carbon	5	⅛W	310
R11	390Ω	Cracked Carbon	5	⅛W	2410
R12	560Ω	Cracked Carbon	5	⅛W	308
R13	3.3k	Cracked Carbon	5	⅛W	1638
R14	2.7k	Cracked Carbon	5	⅛W	311
R15	3.3k	Cracked Carbon	5	⅛W	1638
R16	270Ω	Cracked Carbon	5	⅛W	2716
R17	2.2k	Cracked Carbon	5	⅛W	425
R18	5.6k	Cracked Carbon	5	⅛W	787
R19	1k	Cracked Carbon	5	⅛W	384
R20	1k	Cracked Carbon	5	⅛W	384
R21	3.9k	Cracked Carbon	5	⅛W	312
R22	1k	Cracked Carbon	5	⅛W	384
R23	1k	Cracked Carbon	5	⅛W	384
R24	100Ω	Cracked Carbon	5	⅛W	11504
R25					
R26	10k	Cracked Carbon	5	⅛W	11503
R27	330Ω	Cracked Carbon	5	⅛W	1894
R28	4.7k	Cracked Carbon	5	⅛W	386
R29	470Ω	Cracked Carbon	5	⅛W	1373
R30	4.7Ω	Cracked Carbon	5	⅛W	386
R31	10k	Cracked Carbon	5	⅛W	11503
R32	820Ω	Cracked Carbon	5	⅛W	1637
R33	1.2k	Cracked Carbon	5	⅛W	2087
R34	10Ω	Cracked Carbon	5	⅛W	2259
R35	33Ω	Cracked Carbon	5	⅛W	2931
R36	6.8k	Cracked Carbon	5	⅛W	313
R37	33Ω	Cracked Carbon	5	⅛W	2931
CAPACITORS					
C1	16μF	Electrolytic	-20 +50	350V	25875
C2	32μF	Electrolytic	-20 +50	300V	12189
C3	1000μF	Electrolytic	-10 +50	6.4V	24797
C4	1000μF	Electrolytic	-10 +50	6.4V	24797
C5	.047μF	Ceramic	+80 -20	30V	2793
C6	200μF	Electrolytic	-10 +50	10V	20782
C7	3200μF	Electrolytic	-10 +50	16V	25876
C8	18pF	Ceramic	10	500V	22367
C9	18pf	Ceramic	10	500V	22367
C10	.05μF	Ceramic	20	12V	19657
C11	.05μF	Ceramic	20	12V	19657
C12	470pF	Ceramic	10	500V	22383
C13	18pF	Ceramic	10	500V	22367
C14	1500pF	Ceramic	10	500V	22388
C15	.05μF	Ceramic	20	12V	19657
C16	.05μF	Ceramic	20	12V	19657
C17	60pf swing	Trimmer			30286
C18	1.5-8pF	Trimmer			17998
C19	27pF	Ceramic	20	500V	22369
				0-100pF A.O.T.	
C20	4700pF	Ceramic	25	500V	22393
C21					
C22					
C23	.047μF	Polyester	20	400V	3398
C24	18pF	Ceramic	10	500V	22367
C25	400μF	Electrolytic	-10 +50	25V	20784
C26	.05μF	Ceramic	20	12V	19657
C27	0.1μF	Lemlac		30V	19647
TRANSISTORS					
TR2		2N 3053 (CV8890)			4039
TR3		2N 930 (CV7493)			21548
TR4		BSX 20 (CV7555)			23307
TR5		BSX 20 (CV7555)			23307
TR6		BSX 20 (CV7555)			23307
TR7		BSX 20 (CV7555)			23307
TR8		BSX 20 (CV7555)			23307
TR9		BSX 20 (CV7555)			23307
TR10		BSX 20 (CV7555)			23307
TR11		BSX 20 (CV7555)			23307
TR12		BSX 20 (CV7555)			23307
INTEGRATED CIRCUITS					
IC1		Decade 6995879			25873
IC2		Decade 6995879			25873
IC3		Decade 6995879			25873
IC4		Decade 6995879			25873
IC5		Decade 6995879			25873
IC6		Decade 6995879			25873
IC7		Decade 6995879			25873
IC8		5992729			24094
IC9		5991429			24091
DIODES					
D1		CV 7356			30807
D2					
D3		1N 4003		50V	23642
D4		1N 4003		50V	23642
D5	4.3V	Zener (CV 7141)	5	400mW	27320
D6	20V	Zener (CV 9084)	5	400mW	19955
D7		1N 914 (CV 7367)			23802
D8		1N 4003		50V	23642
MISCELLANEOUS					
XL1		Crystal 1MHz			22350

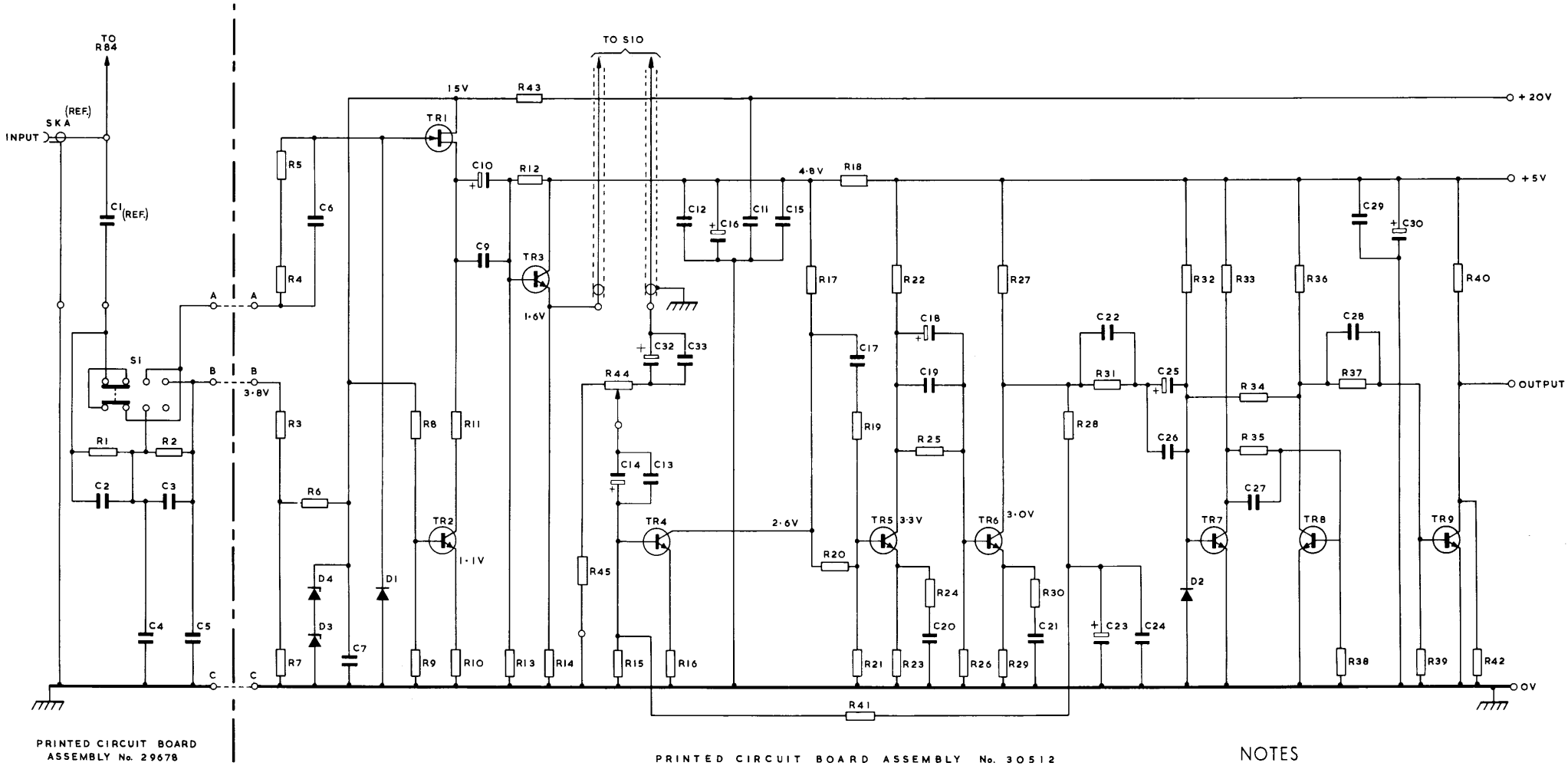

PRINTED CIRCUIT BOARD ASSEMBLY No. 30284
+12·5V FROM MR1
12·5V
+200V
175V~
0V
+20V OUTPUT
+3·8V OUTPUT
RESET PULSE IN
TB INPUT
+5·4V OUTPUT
+4·3V
+4·2V
0·7V
+5V OUTPU
TEST LINK 1
0V
1MHz OUTPUT
STD INPUT
1µS
A.O.T
CRYSTAL OVEN
12V~
+16V OUTPUT
100µS
1mS
10mS
100mS
1 SEC
10 SEC
U.T.S. FROM S1
TIME UNITS
TIME UNITS OUTPUT
GATE TIME OUTPUT
10µS
RESET
COUNT
OV
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
I.C.9
DUAL TWO INPUT GATE CIRCUIT
IC.8
QUAD INVERTER CIRCUIT
OUTPUTS
INPUT
IC1 TO IC7
DECADE CIRCUIT
TOP VIEW OF INTEGRATED CIRCUITS

Component List and Illustrations Section 6

ATTENUATOR AND AMPLIFIER ASSEMBLY

Ref	Value	Description	Tol %		Part No.
RESISTORS					
R1	1M	Carbon	10	250V AC rating	1171
R2	100k	Cracked Carbon	5	1/8W	319
R3	5.6k	Cracked Carbon	5	1/8W	787
R4	120k	Cracked Carbon	5	1/8W	5332
R5	120k	Cracked Carbon	5	1/8W	5332
R6	22k	Cracked Carbon	5	1/8W	1544
R7	8.2k	Cracked Carbon	5	1/8W	314
R8	33k	Cracked Carbon	5	1/8W	317
R9	4.7k	Cracked Carbon	5	1/8W	386
R10	1k	Cracked Carbon	5	1/8W	384
R11	1k	Cracked Carbon	5	1/8W	384
R12	6.8k	Cracked Carbon	5	1/8W	313
R13	6.8k	Cracked Carbon	5	1/8W	313
R14	1k	Cracked Carbon	5	1/8W	384
R15	2.2k	Cracked Carbon	5	1/8W	425
R16	33Ω	Cracked Carbon	5	1/8W	2931
R17	330Ω	Cracked Carbon	5	1/8W	1894
R18	27Ω	Cracked Carbon	5	1/8W	724
R19	100Ω	Cracked Carbon	5	1/8W	11504
R20	1.5k	Cracked Carbon	5	1/8W	385
R21	820Ω	Cracked Carbon	5	1/8W	1637
R22	330Ω	Cracked Carbon	5	1/8W	1894
R23	33Ω	Cracked Carbon	5	1/8W	2931
R24	15Ω	Cracked Carbon	5	1/8W	2085
R25	1.5k	Cracked Carbon	5	1/8W	385
R26	820	Cracked Carbon	5	1/8W	1637
R27	220	Cracked Carbon	5	1/8W	304
R28	1k	Cracked Carbon	5	1/8W	384
R29	33Ω	Cracked Carbon	5	1/8W	2931
R30	15Ω	Cracked Carbon	5	1/8W	2085
R31	330	Cracked Carbon	5	1/8W	1894
R32	12k	Cracked Carbon	5	1/8W	1685
R33	1k	Cracked Carbon	5	1/8W	384
R34	12k	Cracked Carbon	5	1/8W	1685
R35	12k	Cracked Carbon	5	1/8W	1685
R36	1k	Cracked Carbon	5	1/8W	384
R37	2.7k	Cracked Carbon	5	1/8W	311
R38	12k	Cracked Carbon	5	1/8W	1685
R39	1.8k	Cracked Carbon	5	1/8W	310
R40	470Ω	Cracked Carbon	5	1/8W	1373
R41	2.7k	Cracked Carbon	5	1/8W	311
R42	1.2k	Cracked Carbon	5	1/8W	2087
R43	1.2k	Cracked Carbon	5	1/8W	2087
R44	1k	Potentiometer Erie Erie Type 84	20		A4/29699
R45	10Ω	Cracked Carbon	5	1/8W	2259
CAPACITORS					
C1					
C2	4.7pF	Mica	±½pF		4502
C3	4.7pF	Mica	±½pF		4502
C4	33pF	Mica	5	350V	4779
C5	68pF	Mica	5	350V	4513
C6	100pF	Ceramic Erie 801	10	500V	22376
C7	0.047µF	Ceramic Lemco 1212K	+50 -30	30V	2793
C8					
C9	0.047µF	Ceramic Murata	+50 -30	12V	19657
C10	200µF	Electrolytic	20	10V	20782
C11	0.047µF	Ceramic Murata	+50 -30	30V	2793
C12	0.047µF	Ceramic Murata	+50 -30	12V	19657
C13	0.047µF	Ceramic Murata	+50 -30	12V	19657
C14	320µF	Electrolytic	20	6.4V	23591
C15	0.047µF	Ceramic	+50 -30	12V	19657
C16	1000µF	Electrolytic	20	6.4V	24797
C17	15pF	Ceramic	10	500V	22366
C18	200µF	Electrolytic	20	10V	20782
C19	0.047µF	Ceramic Murata	+50 -30	12V	19657
C20	120pF	Disc Erie 801	10	500V	22377
C21	150pF	Disc Erie 801	10	500V	22378
C22	68pF	Disc Erie 801	10	500V	22374
C23	1000µF	Electrolytic	20	6.4V	24797
C24	0.047µF	Ceramic Murata	+50 -30	12V	19657
C25	320µF	Electrolytic	20	6.4V	23591
C26	0.047µF	Ceramic	+50 -30	12V	19657
C27	18pF	Ceramic Eric 801	10	500V	22367
C28	15pF	Ceramic Erie			
C27	18pF	Ceramic Erie 801	10	500V	22367
C28	15pF	Ceramic Erie 801	10	500V	22366
C29	0.047µF	Ceramic Murata	+50 -30	12V	19657
C30	1000µF	Electrolytic	20	6.4V	24797
C31					
C32	320µF	Electrolytic	20	6.4V	23591
C33	0.047µF	Ceramic	+50 -30	12V	19657

Ref	Value	Description			Part No.
TRANSISTORS					
TR1		BFW 11			30526
TR2		BSX 20 (CV 7555)			23307
TR3		BSX 20 (CV 7555)			23307
TR4		BSX 20 (CV 7555)			23307
TR5		BSX 20 (CV 7555)			23307
TR6		BSX 20 (CV 7555)			23307
TR7		BSX 20 (CV 7555)			23307
TR8		BSX 20 (CV 7555)			23307
TR9		BSX 20 (CV 7555)			23307
MISCELLANEOUS					
S1		Switch Slider DP/DT Aeriel Pressings			25869
D1		1N 916 (CV 7368)			1949
D2		1N 914 (CV 7367)			23802
D3	75V	Zener (CV 7104)	5	400mW	22173
D4	75V	Zener (CV 7104)	5	400mW	22173



NOTES

1. SKA AND C1 ARE CALLED FOR ON INTERCONNECTION DIAGRAM. DRAWING No. AO/SK 2273.
2. S1 IS SHOWN IN 10mV POSITION.

Fig. 3 INPUT AMPLIFIER CIRCUIT DIAGRAM AO/SK 2271

Component List and Illustrations Section 6

Ref	Value	Description	Tol %	Part No.
DECADE & DISPLAY CIRCUIT (cont.)				
C38	0.047μF	Ceramic Erie Transcap	+50 -30	12V 19657
C39	0.047μF	Ceramic Erie Transcap	+50 -30	12V 19657
C40	18pF	Ceramic Erie 801	±10	500V 22367
C41	0.047μF	Ceramic Erie Transcap	+50 -30	12V 19657
C42	0.047μF	Ceramic Erie Transcap	+50 -30	12V 19657
C43	0.047μF	Ceramic Erie Transcap	+50 -30	12V 19657
TRANSISTORS				
TR1		BSX 20 (CV 7555)		23307
TR2		BSX 20 (CV 7555)		23307
TR3		BSX 20 (CV 7555)		23307
TR4		BSX 20 (CV 7555)		23307
TR5		BSX 20 (CV 7555)		23307
TR6		BSX 20 (CV 7555)		23307
TR7		BSX 20 (CV 7555)		23307
TR8		BSX 20 (CV 7555)		23307
TR9		BSX 20 (CV 7555)		23307
TR10		BSX 20 (CV 7555)		23307
TR11		BSX 20 (CV 7555)		23307
TR12		BSX 20 (CV 7555)		23307
TR13		BSX 20 (CV 7555)		23307
TR14		BSX 20 (CV 7555)		23307
TR15		BSX 20 (CV 7555)		23307
TR16		V405A (CV 7594)		19689
TR17		BCY 70 (CV 9023)		23354
TR18		BFW 11		30526
TR19		BSX 20 (CV 7555)		23307
TR20		BCY 70 (CV 9023)		23354
TR21		BSX 20 (CV 7555)		23307
TR22		BSX 20 (CV 7555)		23307
TR23		BSX 20 (CV 7555)		23307
TR24		V405A (CV 7594)		19689
TR25		BSX 20 (CV 7555)		23307
DIODES				
D1		1N 4148(CV 7367)		23802
D4		1N 4148(CV 7367		23802
D5		1N 4148(CV 7367)		23802
D8		1N 4148(CV 7367)		23802
D9		1N 4148(CV 7367)		23802
D11		1N 4148(CV 7367)		23802
D13		1N 4148(CV 7367)		23802
D16		1N 4148(CV 7367)		23802
D17		1N 4148(CV 7367)		23802
D18		1N 4148(CV 7367)		23802
INTEGRATED CIRCUITS				
IC1		59-926-29P		24090
IC2		59-926-29P		24090
IC3		69-958-79		25873
IC4		69-958-79		25873
IC5		69-958-79		25873
IC6		69-958-79		25873
IC7		59-960-79		24096
IC8		59-960-79		24096
IC9		59-960-79		24096
IC10		59-960-79		24096
IC11		59-960-79		24096
IC12		59-960-79		24096
IC13		59-959-79		24095
IC14		59-959-79		24095
IC15		59-959-79		24095
IC16		59-959-79		24095
IC17		59-959-79		24095
IC18		59-959-79		24095
IC19		59-926-29P		24090
IC20		59-926-29P		24090
IC21		59-914-29P		24091
IC22		59-926-29P		24090
IC23		59-914-29P		24091
IC24		59-926-29P		24090
MISCELLANEOUS				
ILP1		ZM 1175 Mullard	Numerical	28127
ILP2		ZM 1175 Mullard	Indicator Tube Neon	28127
ILP3		ZM 1175 Mullard		28127
ILP4		ZM 1175 Mullard		28127
ILP5		ZM 1175 Mullard		28127
ILP6		ZM 1175 Mullard		28127

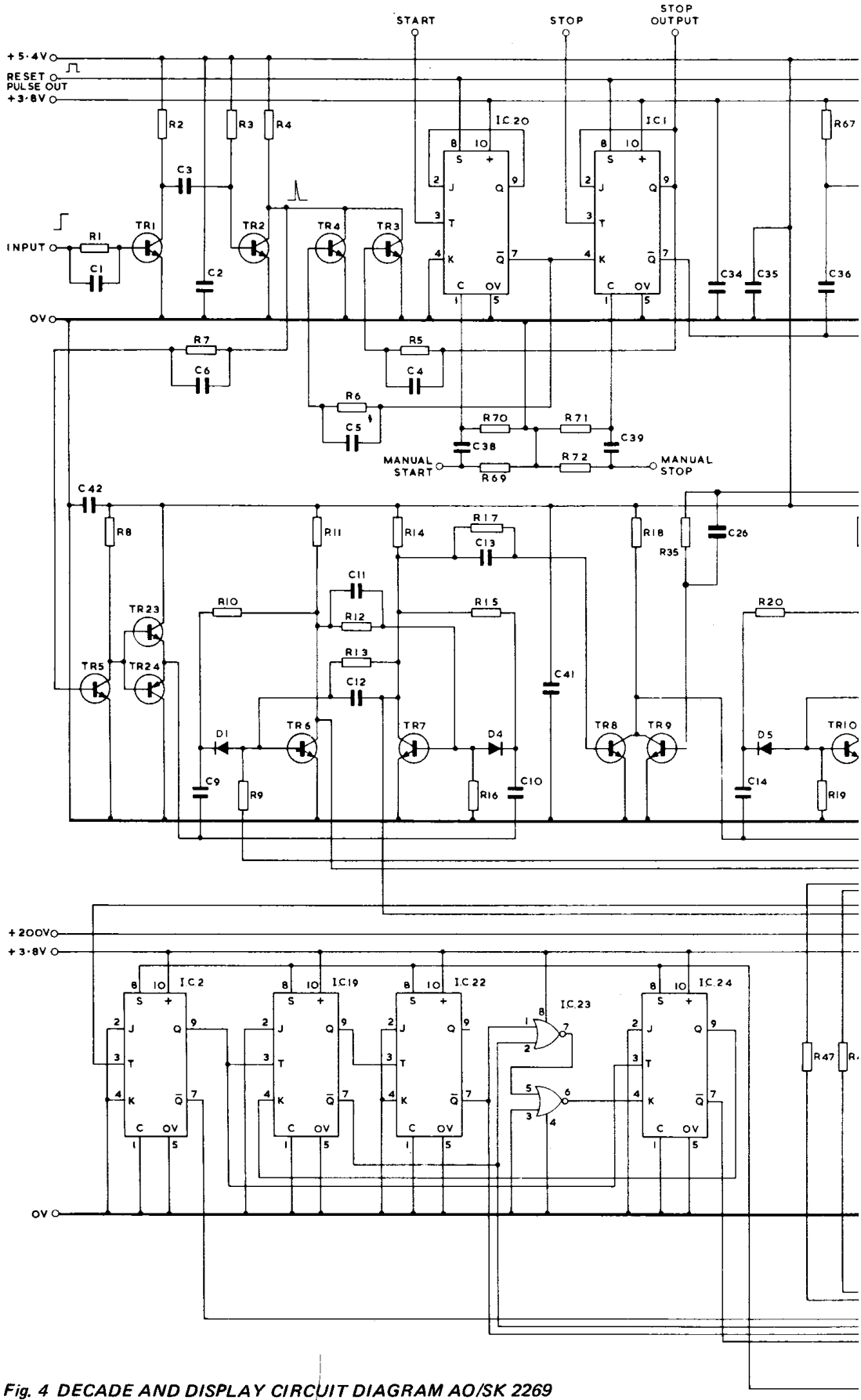
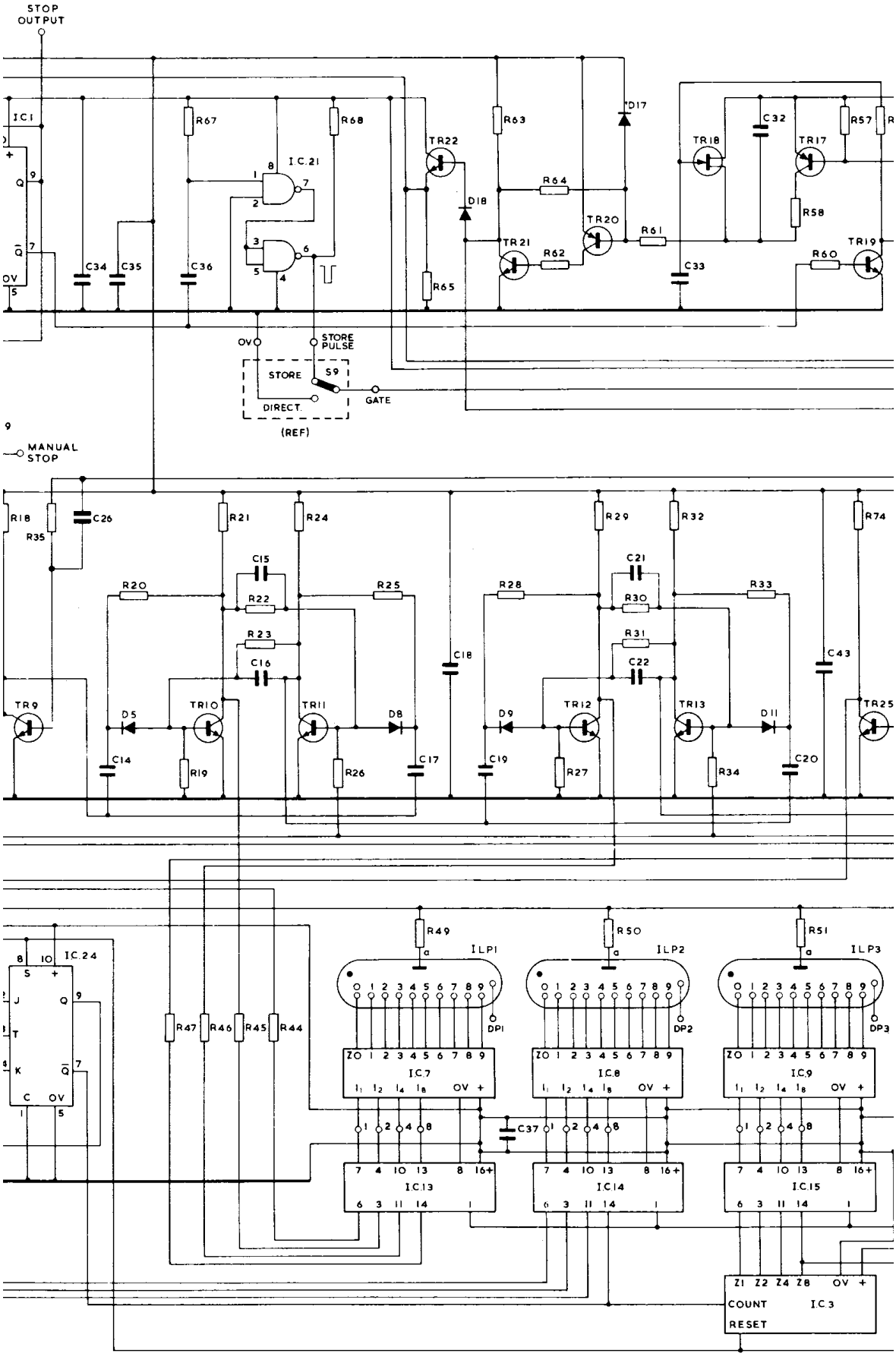
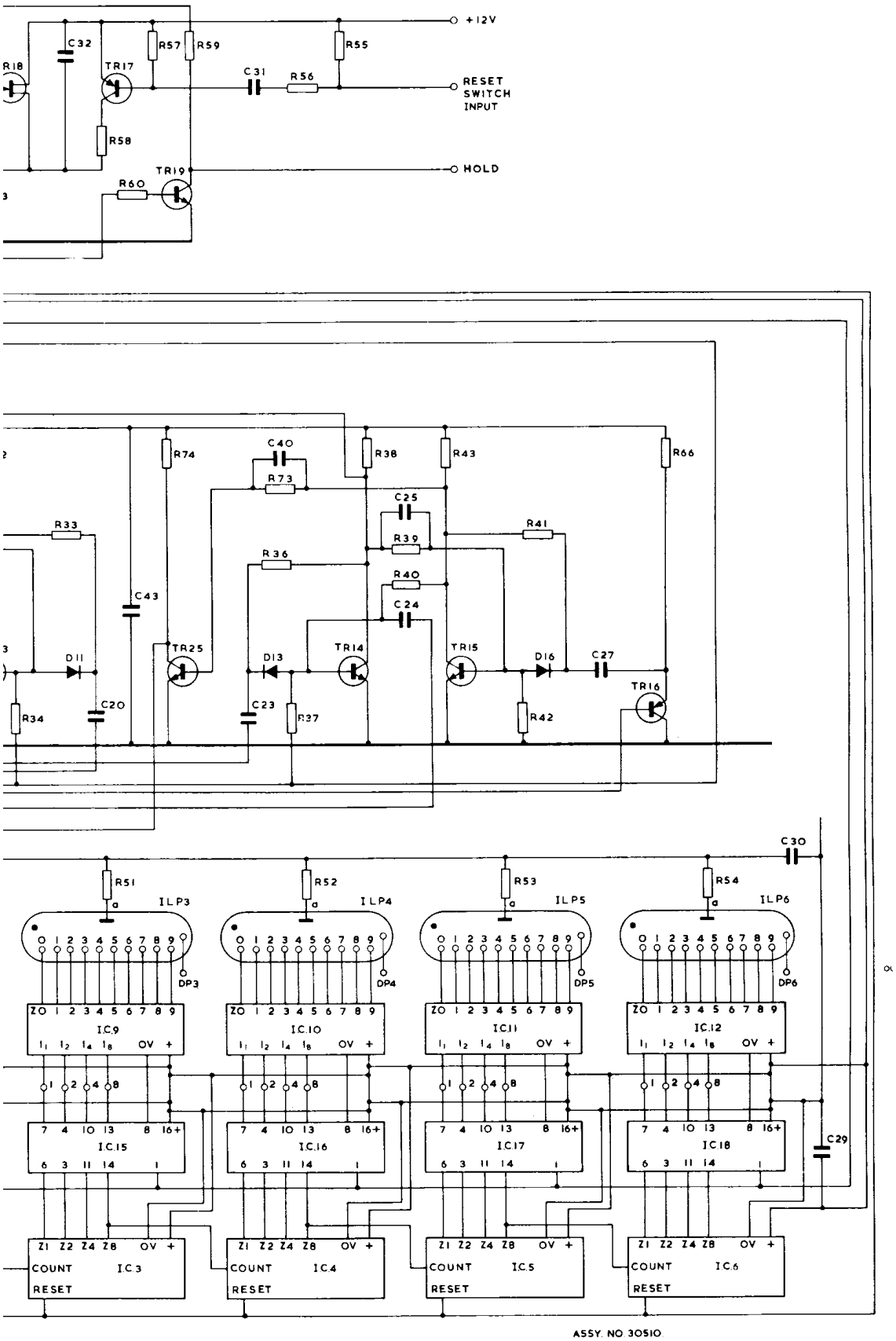


Fig. 4 DECADE AND DISPLAY CIRCUIT DIAGRAM AO/SK 2269


STOP OUTPUT
IC1
R67
R68
I.C.21
TR22
R63
D17
TR18
C32
TR17
R57
R64
D18
R58
TR20
R61
TR21
R62
TR19
R60
C34
C35
C36
R65
C33
OV
STORE PULSE
STORE
S9
DIRECT.
GATE
(REF)
MANUAL STOP
R18
R35
C26
R21
R24
R29
R32
R74
C15
R20
R25
R28
C21
R33
R22
R30
R23
R31
C18
C43
C16
C22
TR9
D5
TR10
TR11
D8
D9
TR12
TR13
D11
TR25
C14
R19
R26
C17
C19
R27
R34
C20
IC.24
R49
R50
R51
ILP1
ILP2
ILP3
R47
R46
R45
R44
DP1
DP2
DP3
IC.7
IC.8
IC.9
C37
IC.13
IC.14
IC.15
COUNT
RESET
IC.3

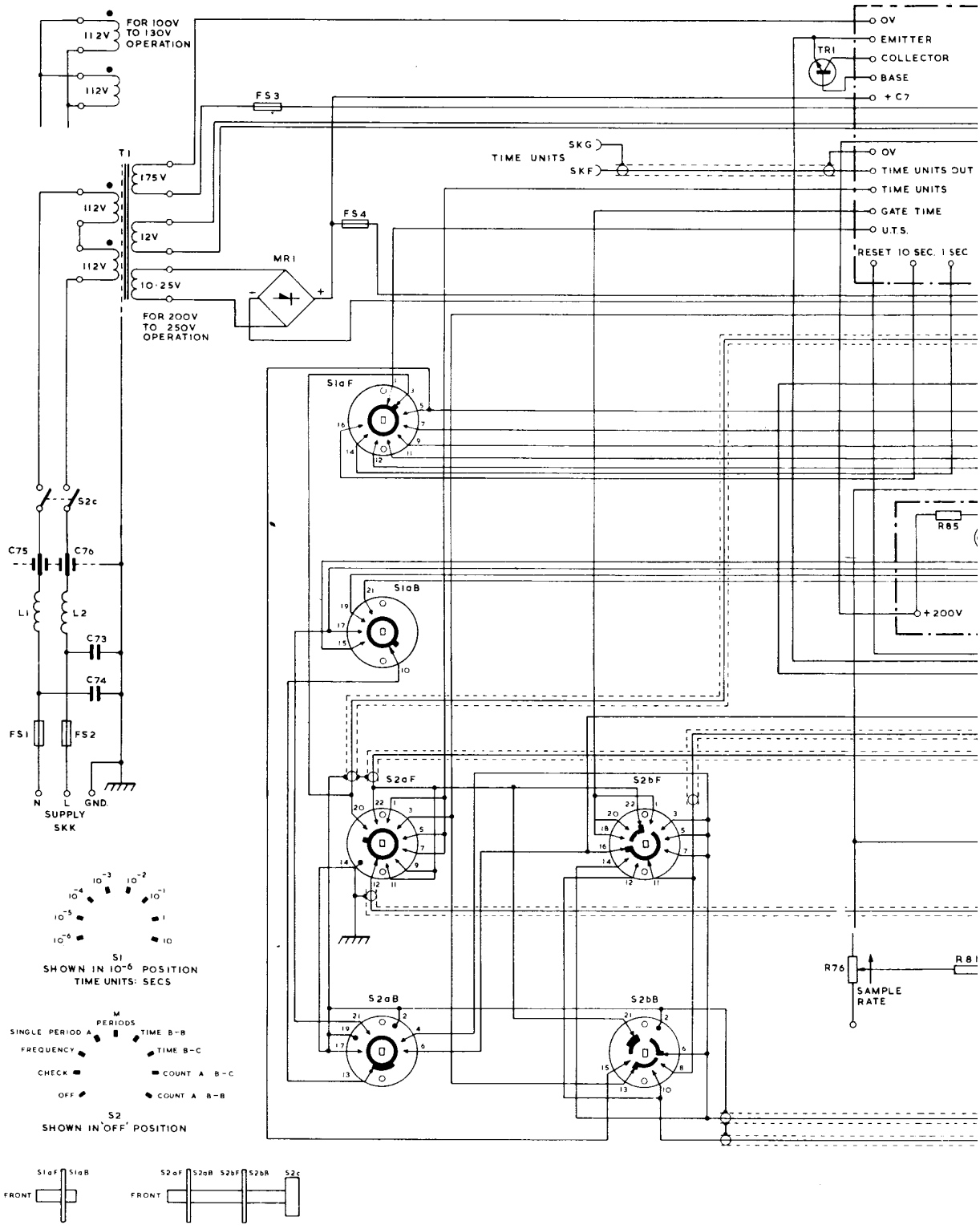

+12V
RESET SWITCH INPUT
HOLD
C32
R57
R59
R55
TR17
C31
R56
R18
R58
TR19
R60
R74
C40
R38
R43
R66
R73
C25
R41
R33
R39
R36
R40
C43
C24
TR25
TR14
TR15
D11
D13
D16
C27
TR16
C20
C23
R37
R34
R42
C30
R51
R52
R53
R54
ILP3
ILP4
ILP5
ILP6
DP3
DP4
DP5
DP6
IC.9
IC.10
IC.11
IC.12
IC.15
IC.16
IC.17
IC.18
C29
COUNT
RESET
IC.3
IC.4
IC.5
IC.6
ASSY. NO. 30510

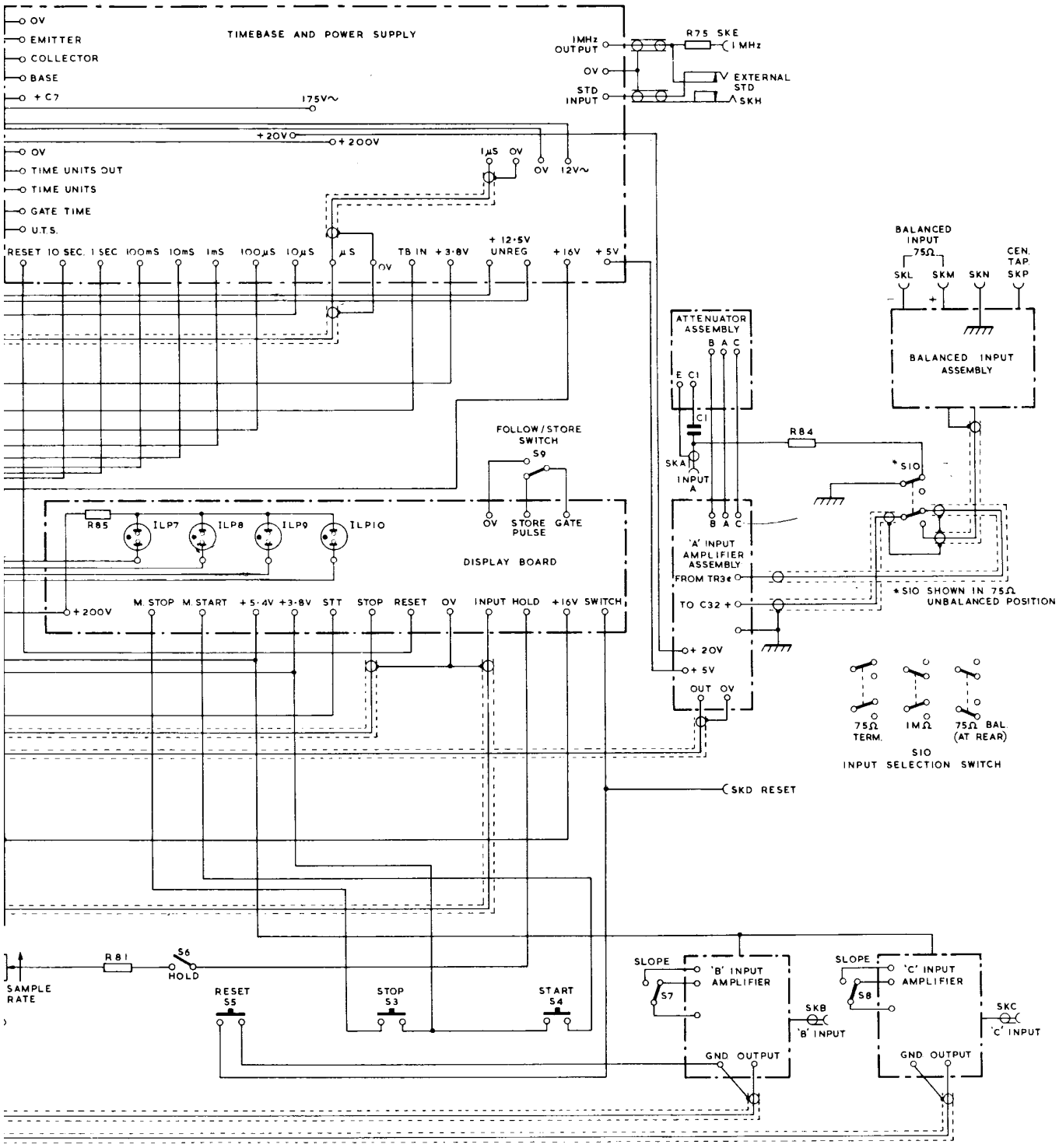
Component List and Illustrations Section 6

INTERCONNECTION DIAGRAM

Ref	Value	Description	Tol %		Part No.
RESISTORS					
R75	2.7k	Cracked Carbon	±5	1/8W	311
R76	5M Rev. Log.	Control Pot A.B. AY45	Including S6		25877
R81	10k	Cracked Carbon	±5	1/8W	11503
R84	75Ω	Metal Film	±2	½W	28780
R85	270k	Cracked Carbon	±5	1/8W	1679
CAPACITORS					
C1	0.15μF	Tropyfol 'M'	10	400V	2366
C73	5000pF	Erie K350011/C08	-20 +80	3KV	1514
C74	5000pF	Erie K350011/C08	-20 +80	3KV	1514
C75	1000pF	Cap.Feed Thro' Erie K2600/361	-20 +80	500V	3313
C76	1000pF	Cap.Feed Thro' Erie K2600/361	-20 +80	500V	3313
SWITCHES					
S1		Time Units			25664
S2		Function			25665
S3		PBS1M Rendar			4881
S4		PBS1M Rendar			4881
S5		PBS1M Rendar			4881
S6		Part of R76			
S7		Ariel Pressings Slider 2P2W A/P RA2302			24545
S8		Slider 2P2W A/P RA2302			24545
S9		SP/DT MST 105D Waycom			23995-
S10		DP/DT MST 205PA			27816

Ref	Value	Description	Tol %	Part No.
SOCKETS				
SKA		Connector Plug No. 1		30498
SKB		Connector Plug No. 1		30498
SKC		Connector Plug No. 1		30498
SKD		B/L E6013 4mm Black		25675
SKE		B/L E6013 4mm Black		25675
SKF		B/L E6013 4mm Black		25675
SKG		B/L E6013 4mm Black		25675
SKH		Rendar MJ600/A		2726
SKK		Bulgin P429		4478
FUSES				
FS1		Belling Lee L562	2.5A	21189
FS2		Belling Lee L562	2.5A	21189
FS3		Belling Lee L562	100mA	4876
FS4		Belling Lee L754	2A	1255
MISCELLANEOUS				
TR1		2N3055 (CV 8889, 9195)		3813
MR2		Bridge Rectifier VS 248 2 Amp		26784
ILP7		Indicator Neon Hivac 3L		12781
ILP8		Indicator Neon Hivac 3L		12781
ILP9		Indicator Neon Hivac 3L		12781
ILP10		Indicator Neon Hivac 3L		12781
T1		Transformer		MT660
L1		Choke 1A Dubilier 666		11212
L2		Choke 1A Dubilier 666		11212


FOR 100V TO 130V OPERATION
112V
112V
T1
175V
112V
12V
112V
10·25V
FOR 200V TO 250V OPERATION
FS3
FS4
MR1
SKG
TIME UNITS
SKF
TR1
OV
EMITTER
COLLECTOR
BASE
+C7
OV
TIME UNITS OUT
TIME UNITS
GATE TIME
U.T.S.
RESET 10 SEC. 1 SEC
S1aF
S1aB
S2aF
S2bF
S2aB
S2bB
S2c
C75
C76
L1
L2
C73
C74
FS1
FS2
N
L
GND.
SUPPLY
SKK
R85
+200V
R76
R81
SAMPLE RATE
S1
SHOWN IN 10⁻⁶ POSITION
TIME UNITS: SECS
S2
SHOWN IN 'OFF' POSITION
SINGLE PERIOD A
M PERIODS
TIME B-B
FREQUENCY
TIME B-C
CHECK
COUNT A B-C
OFF
COUNT A B-B
FRONT
FRONT


TIMEBASE AND POWER SUPPLY
OV
EMITTER
COLLECTOR
BASE
+ C7
175V~
+20V
+200V
OV
TIME UNITS OUT
TIME UNITS
GATE TIME
U.T.S.
RESET 10 SEC. 1 SEC 100mS 10mS 1mS 100µS 10µS µS OV TB IN +3·8V + 12·5V UNREG +16V +5V
1µS OV
OV 12V~
1MHz OUTPUT
OV
STD INPUT
R75 SKE
1 MHz
EXTERNAL STD SKH
FOLLOW/STORE SWITCH
S9
OV STORE PULSE GATE
R85
ILP7 ILP8 ILP9 ILP10
DISPLAY BOARD
+200V
M. STOP M. START +5·4V +3·8V STT STOP RESET OV INPUT HOLD +16V SWITCH
ATTENUATOR ASSEMBLY
B A C
E C1
C1
R84
SKA
INPUT A
'A' INPUT AMPLIFIER ASSEMBLY
FROM TR3e
TO C32 +
+20V
+5V
OUT OV
BALANCED INPUT 75Ω
CEN. TAP
SKL SKM SKN SKP
BALANCED INPUT ASSEMBLY
*S10
*S10 SHOWN IN 75Ω UNBALANCED POSITION
75Ω TERM.
1MΩ
75Ω BAL. (AT REAR)
S10 INPUT SELECTION SWITCH
SKD RESET
SAMPLE RATE
R81
S6 HOLD
RESET S5
STOP S3
START S4
SLOPE
'B' INPUT AMPLIFIER
S7
SKB 'B' INPUT
GND OUTPUT
SLOPE
'C' INPUT AMPLIFIER
S8
SKC 'C' INPUT
GND OUTPUT

Component List and Illustrations Section 6

B & C INPUT AMPLIFIER CIRCUIT

Ref	Value	Description	Tol %		Part No.
RESISTORS					
R1	47kΩ	Cracked Carbon	5	1/8W	318
R2	39kΩ	Cracked Carbon	5	1/8W	1639
R3	680Ω	Cracked Carbon	5	1/8W	309
R4	33kΩ	Cracked Carbon	5	1/8W	317
R5	2.7Ω	Cracked Carbon	5	1/8W	311
R6	470Ω	Cracked Carbon	5	1/8W	1373
R7	10kΩ	Cracked Carbon	5	1/8W	11503
R8	27kΩ	Cracked Carbon	5	1/8W	316
R9	560Ω	Cracked Carbon	5	1/8W	308
R10	3.9kΩ	Cracked Carbon	5	1/8W	312
R11	33kΩ	Cracked Carbon	5	1/8W	317
R12	4.7kΩ	Cracked Carbon	5	1/8W	386
R13	1kΩ	Cracked Carbon	5	1/8W	384
R14	47kΩ	Cracked Carbon	5	1/8W	318
R15	39kΩ	Cracked Carbon	5	1/8W	1639
R16	680Ω	Cracked Carbon	5	1/8W	309
R17	33kΩ	Cracked Carbon	5	1/8W	317
R18	2.7kΩ	Cracked Carbon	5	1/8W	311
R19	470Ω	Cracked Carbon	5	1/8W	1373
R20	10kΩ	Cracked Carbon	5	1/8W	11503
R21	27kΩ	Cracked Carbon	5	1/8W	316
R22	560Ω	Cracked Carbon	5	1/8W	308
R23	3.9kΩ	Cracked Carbon	5	1/8W	312
R24	33kΩ	Cracked Carbon	5	1/8W	317
R25	4.7kΩ	Cracked Carbon	5	1/8W	386
R26	1kΩ	Cracked Carbon	5	1/8W	384
R27	68Ω	Cracked Carbon	5	1/8W	1640

Ref	Value	Description	Tol %		Part No.
CAPACITORS					
C1	0.047μF	Erie Transcap	+50 -30	12V	19657
C2	0.15μF	Polyester Film	10	160V	4538
C3	12.5μF	C426 Mullard Electrolytic	-10 +50	25V	20775
C4	18pF	Ceramic Erie 801	10	500V	22367
C5	18pF	Ceramic Erie 801	10	500V	22367
C6	0.1μF	Erie	+80 -20	30V	19647
C7	0.15μF	Polyester Film	10	160V	4538
C8	12.5μF	C426 Mullard Electrolytic	-10 +50	25V	20775
C9	18pF	Ceramic Erie 801	10	500V	22367
C10	18pF	Ceramic Erie 801	10	500V	22367
C11	320μF	C426 Mullard Electrolytic	-10 +50	6.4V	23591
TRANSISTORS					
TR1		BC 108 (CV10440)			26110
TR2		BSX20 (CV 7555)			23307
TR3		BSX20 (CV 7555)			23307
TR4		BC 108 (CV10440)			26110
TR5		BSX20 (CV 7555)			23307
TR6		BSX20 (CV 7555)			23307
DIODES					
D1		1N 4148(CV 7367)			23802
D2		1N 4148(CV 7367)			23802

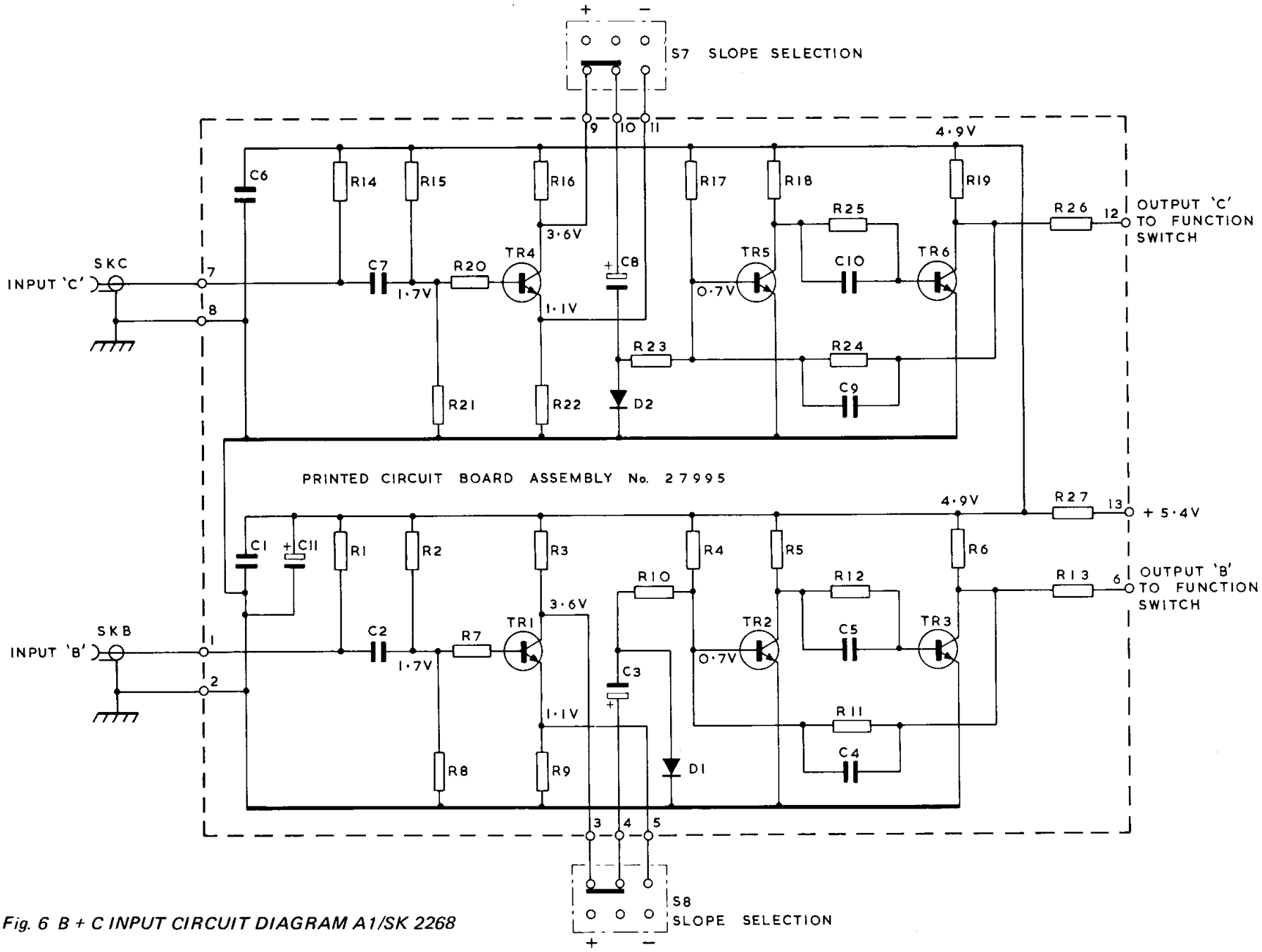
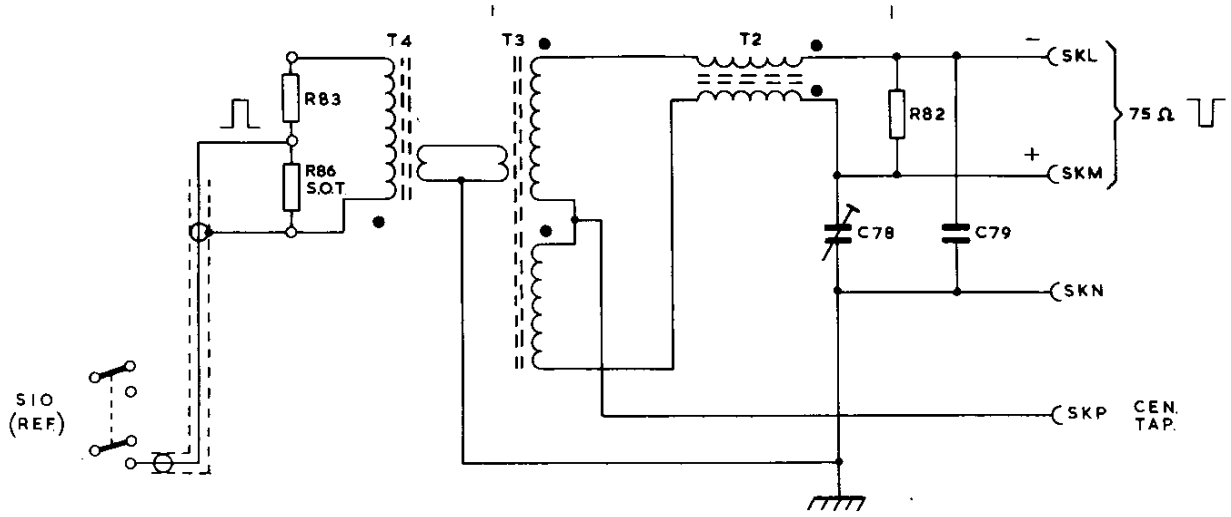


Fig. 6 B + C INPUT CIRCUIT DIAGRAM A1/SK 2268

Component List and Illustrations Section 6

BALANCED INPUT CIRCUIT

Ref	Value	Description	Tol %		Part No.
RESISTORS					
R82	75Ω	Metal Oxide MR5 or TR5	-2	½W	28780
R83	1.2k	Cracked Carbon	-5	1/8W	2087
R86	4.7k	Cracked Carbon 1.5K–4.7K S.O.T.	5	1/8W	386
CAPACITORS					
C78	1 5/8 pF	Trimmer Lemco	-25 +50	500V	17998
C79	4.7pF	Ceramic	±1pF	500V	29649
MISCELLANEOUS					
T2 T3 T4		Toroid Windings on S.T.C. Core Type CRO71/12A/A/SA601			A2/30199 A4/30201
SKL		Connector 1/SSO/14			30203
SKM		Connector 1/SSO/14			30203
SKN		Connector 1/SSO/14			30203
SKP		Connector 1/SSO/14			30203



ASSY No. 30195

Fig. 7 BALANCED INPUT CIRCUIT DIAGRAM A2/SK 2272

Component List and Illustrations Section 6

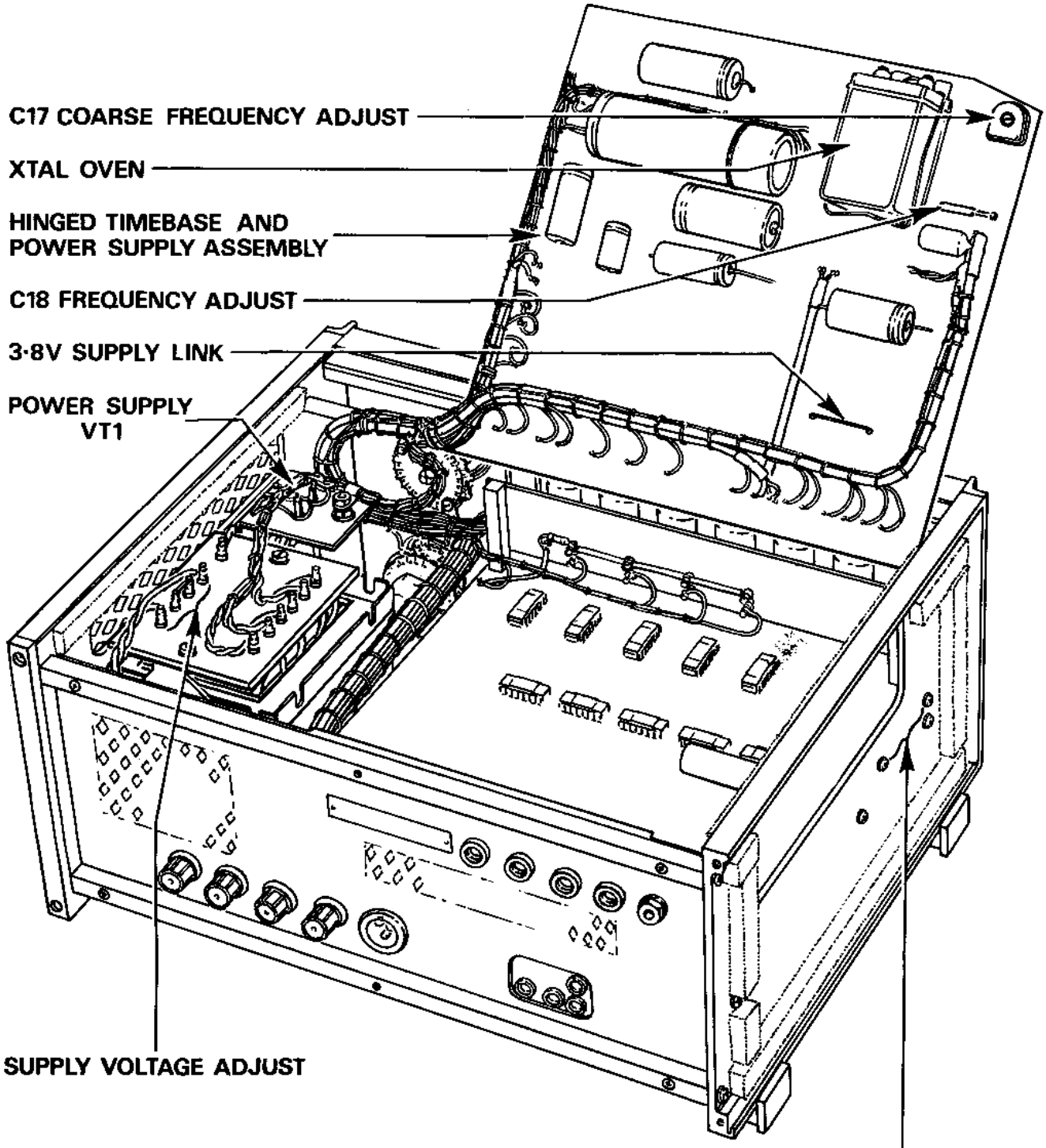


Fig. 8 COMPONENT LAYOUT (TOP VIEW)

Component List and Illustrations Section 6

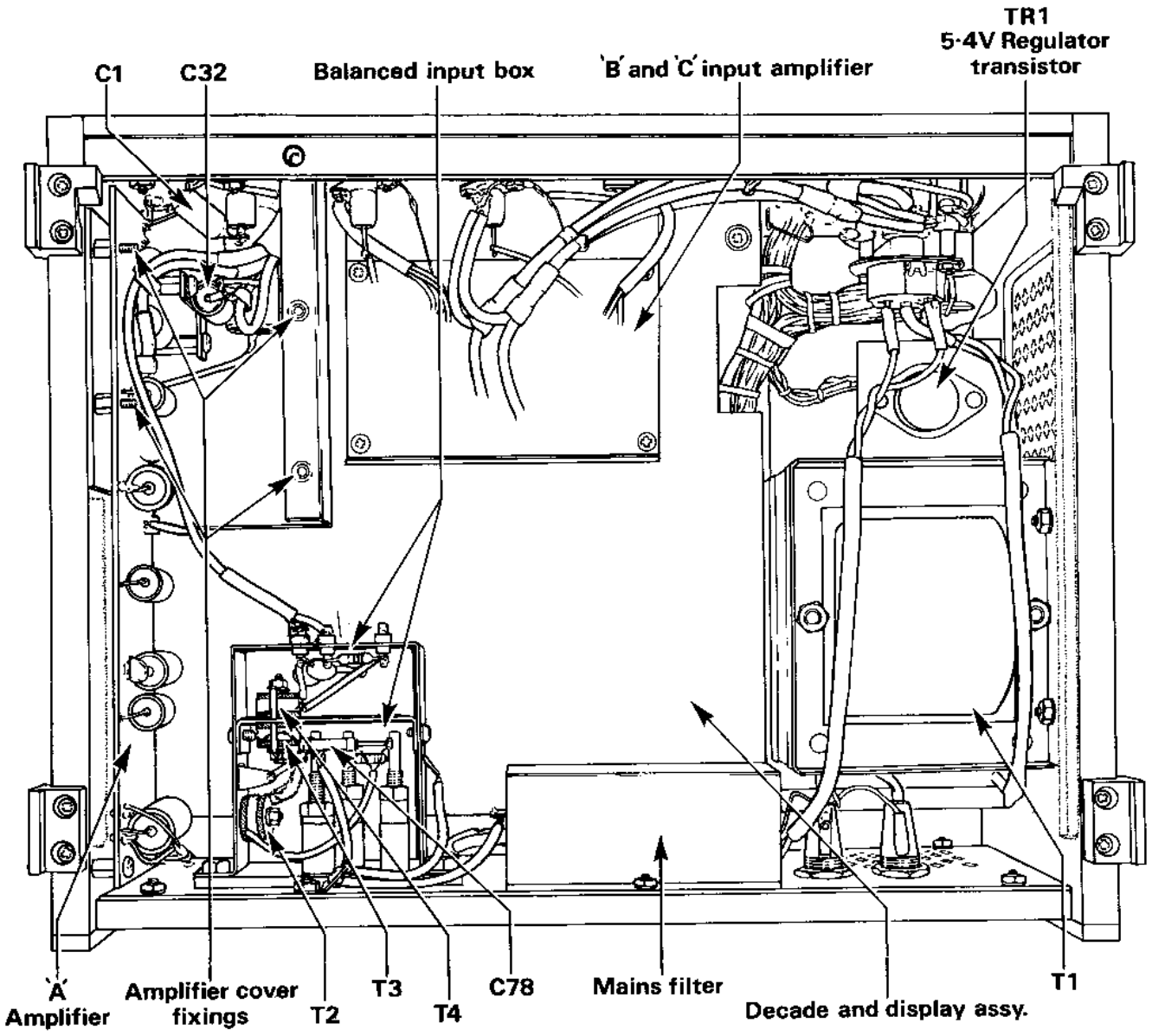


Fig. 9 COMPONENT LAYOUT (UNDERSIDE VIEW)